Static Noise Margin Analysis of SRAM Cell for High Speed Application

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Abstract

This paper presents the different types of analysis such as noise, voltage, read margin and write margin of Static Random Access Memory (SRAM) cell for high-speed application. The design is based upon the 0.18 µm CMOS process technology. Static Noise Margin (SNM) is the most important parameter for memory design. SNM, which affects both read and write margin, is related to the threshold voltages of the NMOS and PMOS devices of the SRAM cell that is why we have analyzed SNM with the Read Margin, Write Margin and also the Threshold voltage. For demand of the high-speed application of the SRAM cell operation, supply voltage scaling is often used that is why we have done Data Retention Voltage. We took different types of curve by which straightforwardly we could analyses the size of the transistor of the SRAM cell for high-speed application.

Keywords: *Static Noise Margin, SRAM, VLSI, CMOS.*

1. Introduction

This paper is to introduce how the speed of the SRAM cell depends on the different types of noise analysis. Both cell ratio and pull-up ratio are important parameters because these are the only parameters in the hand of the design engineer [1]. Technology is getting more complex day by day. Presently in industry, 32 nm CMOS process technology is used. So it should be carefully selected in the design of the memory cell. There are number of design criteria that must be taken into the consideration. The two basic criteria which we have taken such as one is the data read operation should not be destructive and another one is static noise margin should be in the acceptable range [3]. For demand of the high speed SRAM cell operation, supply voltage scaling is often used. Therefore, the analysis of SRAM read/write margin is essential for high speed SRAMs.

A key insight of this paper is that we can analyze different types of noise margin for high speed SRAM cell. We evaluate the different of curve with respect to the all of them. And finally we can conclude how the different type of noise margin affects the speed of the SRAM cell.

We first reviewed existing approaches for static noise margin, data retention voltage, read margin and write margin. Then we have done the comparison of all of them with different aspects.

2. Static Noise Margin

In this section, first we introduce existing static approach that is butterfly method for measuring static noise margin [1]. Static noise margin of the SRAM cell depends on the cell ratio (CR), supply voltage and also pull up ratio. For stability of the SRAM cell, good SNM is required that is depends on the value of the cell ratio, pull up ratio and also for supply voltage. Driver transistor is responsible for 70 % value of the SNM [3].

Cell ratio is the ratio between sizes of the driver transistor to the load transistor during the read operation [1]. Pull up ratio is also nothing but a ratio between sizes of the load transistor to the access transistor during write operation [1]. The basic circuit of SRAM cell is shown in given below as figure 1.

CR= (W1/L1) / (W5/L5) (During Read Operation)
PR = (W4/L4) / (W6/L6) (During Write Operation)

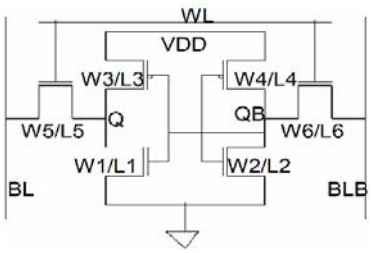
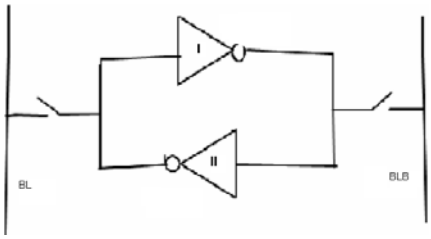


Fig. 1 Circuit for basic SRAM cell [1].

SNM, which affects both read margin and write margin, is related to the threshold voltages of the NMOS and PMOS devices in SRAM cells [3]. Typically, to increase the SNM, the threshold voltages of the NMOS and PMOS devices need to be increased. However, the increase in threshold voltage of PMOS and NMOS devices is limited. The reason is that SRAM cells with MOS devices having too high threshold voltages are difficult to operate; as it is hard to flip the operation of MOS devices.

Changing the Cell Ratio, we got different speed of SRAM cell. If cell ratio increases, then size of the driver transistor also increases, for hence current also increases. As current is an increase, the speed of the SRAM cell also increases. By changing the Cell ratio we got corresponding SNM. For different values of CR, we got different values of SNM in different technology of SRAM cell. This is same for DRV vs. SNM.

Adobe Photoshop CS3 tool was used for rotation purpose. We have done this project by Tanner 13.1 version tool. Practically we can't get butterfly structure that is why we rotated the graph according to x-y coordinates. Finally we got butterfly structure as shown in figure 2a. Since by knowing the diagonals of the maximum embedded squares we can calculate the sides. The squares have maximum size when the lengths of their diagonal D1 and D2 are maximum; the extremes of this curve correspond to the diagonals of the maximum embedded squares.



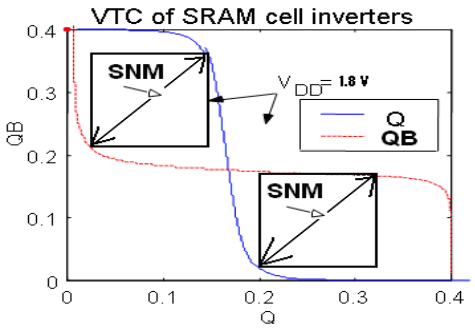


Fig. 2a Circuit for two cross couple inverter with BL and BLB [1].

Fig. 2b Circuit for the calculation of SNM after rotation [1].

3. Data Retention Voltage

Data Retention Voltage (Vdr): Min. power supply voltage to retain high node data in the standby mode [1]. There are two nodes (q and qb) of the SRAM cell for storing value either 0 or 1. Then decrease the power supply voltage until the flip the state of SRAM cell or content of the SRAM cell remain constant. Vdd scales down to DRV, the Voltage Transfer Curves (VTC) of the internal inverters degrade to such a level that Static Noise Margin (SNM) of the SRAM cell reduces to zero.

If Q=1, Q'=0, it is changes the value of Q=0, Q'=1 after decreasing the value of the power supply voltage. Data retention voltage should be greater than threshold voltage. We took the value of power supply voltage upto 0.6V then it is change the state of cell. We know, minimum power supply voltage to retain high node data in the standby mode: Vdr=Vdd=0.6V for 180 nm Technology that is data retention voltage.

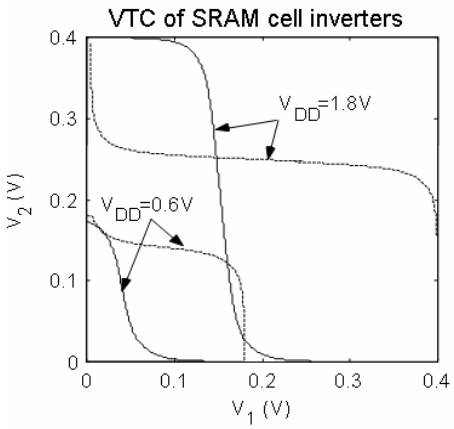


Fig. 3 VTC of SRAM cell during DRV calculation[1].

4. Write Margin

Write margin is defined as the minimum bit line voltage required to flip the state of an SRAM cell [1]. The write margin value and variation is a function of the cell design, SRAM array size and process variation.

Already five existing static approaches for measuring write margin are available [5]. First we calculated write margin by the existing bl sweeping method then we compared that with Static Noise Margin.

Write margin is directly proportional to the pull up ratio. Write margin increases with the increases value of the pull up ratio. So carefully you have to design SRAM cell inverters before calculating the write margin of SRAM cell during write operation. Pull up ratio also fully depends on the size of the transistor.

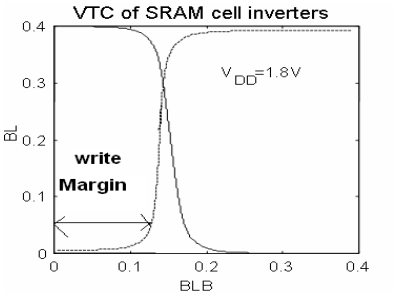


Fig. 4a VTC of SRAM cell to get write margin calculation by the BL sweeping method [5].

5. Read Margin

Based on the VTCs, we define the read margin to characterize the SRAM cell's read stability. We calculate the read margin based on the transistor's current model [7]. Experimental results show that the read margin accurately captures the SRAM's read stability as a function of the transistor's threshold voltage and the power supply voltage variations. Below fig.4c shows the read margin of the SRAM cell during read operation.

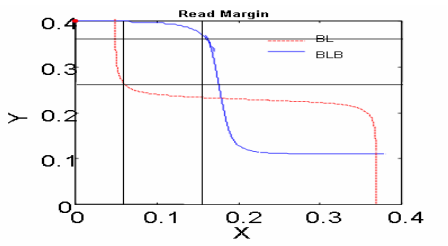


Fig. 4b Shows the read margin [7].

Read margin is directly proportional to the cell ratio. Read margin increases with the increase in value of the pull up ratio. So carefully you have to design SRAM cell inverters before calculating the read margin of SRAM cell during read operation. Pull up ratio also fully depends on the size of the transistor. The process of analysis of read margin is same as the analysis of static noise margin.

6. Simulation Results and Discussion

Some important results that are observed from simulation of the schematic designed in S-Edit are summarized below:

The cell ratio and the pull up ratio of the SRAM cell are given below:
CR= (W1/L1) / (W5/L5) =1(During Read Operation)
PR = (W4/L4) / (W6/L6) =3 (During Write Operation)
The range cell ratio and pull-up ratio should be in 1-2.5 and 3-4 respectively otherwise data will be destroy.

SNM calculation: We have done the SNM calculation by this way with respect of above figure:
Side of the Maximum Square =A=0.209V=209 mV,
Lengths of diagonal of Square (D) = √ 2 * One side of the Square =√ 2 * 209, SNM= D/ √ 2 =√ 2 * 209/√ 2, So SNM =One of the side=A=209 mV.

We have taken of cell ratio vs. static noise margin, then the value of static noise margin increases with the increase of cell ratio of the SRAM cell in 180 nm technology. If the value of the driver transistor is increased then CR is increased. For hence current is increased then speed is also increased.

Table 1: CR vs. SNM

Technology (mm)	CR	SNM(mV)
180 nm	0.8	205
	1.0	209
	1.2	214
	1.4	218
	1.6	223

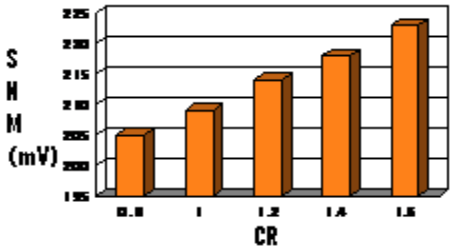


Fig. 5a The graphical representation of CR vs. SNM of the SRAM cell.

The above graph shows SNM increases when CR increases. CR increases means the size of driver transistor increases.

Data Retention Voltage also effects on the SNM of the SRAM cell. It is important parameter for the saving supply voltage. SNM decreases with the decrease in value of the data retention voltage. Data Retention Voltage should be greater than threshold voltage. Data Retention Voltage is greater than the threshold voltage is shown below:

Table 2: DRV vs. SNM

Technology	DRV(V)	SNM(mV)
180nm	1.8	200
	1.6	195
	1.4	191
	1.2	188
	1.0	184
	0.8	180
	0.6	178

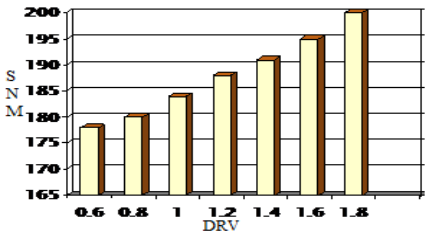


Fig. 5b The graphical representation of DRV vs. SNM of the SRAM cell.

The above graph shows SNM increases when DRV increases. DRV decreases means the voltage also decreases but content of the SRM cell is remaining constant.

Below table shows the read margin vs. SNM. We observed that both read margin and SNM are proportional with respect to the CR.

Table 3: Read Margin vs. SNM

Technology	CR	Read Margin	SNM (mV)
180nm	1.0	0.393	205
	1.2	0.398	209
	1.4	0.401	214
	1.6	0.404	218
	1.8	0.407	223
	2.0	0.409	225

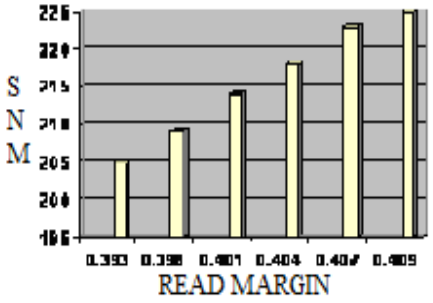


Fig. 5c
The graphical representation of Read Margin vs. SNM of the SRAM cell

The above graph shows SNM increases when read margin increases and read margin increases means the read operation of the SRAM cell will be too good.

Below table shows the write margin vs. SNM. We observed that both write margin and SNM are proportional with respect to the PR.

Table 3: Write Margin vs. SNM

Technology	PR	Write margin	SNM(mV)
180 nm	3.0	0.487	210
	3.2	0.489	213
	3.4	0.491	217
	3.6	0.493	221
	3.8	0.496	223
	4.0	0.498	227

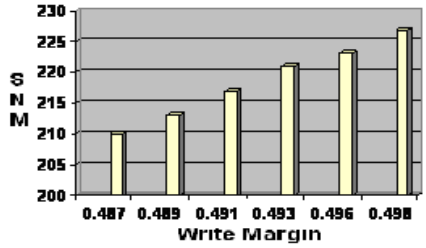


Fig. 5d The graphical representation of Write Margin vs. SNM of the SRAM cell

The above graph shows SNM increases when write margin increases. Write margin increases means the write operation of the SRAM cell will be too good.

Below table shows the threshold voltage vs. SNM. We observed that if the threshold voltage increases the value of the SNM also increases.

Table 4: Threshold Voltage vs. SNM

Technology	Threshold Voltage SNM	SNM (mV)
180 nm	PMOS: -0.3948389 NMOS: 0.3948389	200
	PMOS: -0.6 NMOS: 0.6	205
	PMOS: -0.8 NMOS: 0.8	209
	PMOS: -1.0 NMOS: 1.0	214
	PMOS: -1.2 NMOS: 1.2	218

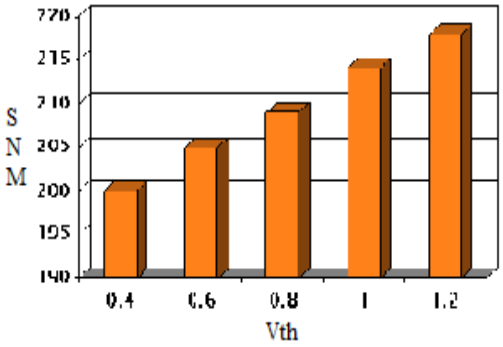


Fig. 5e The graphical representation of threshold voltage vs. SNM of the SRAM cell

The above graph shows SNM is increases when threshold voltage is increases.

7. Conclusion

In this paper, we have analysed Static Noise Margin and then we have compared Static Noise Margin with the Data Retention Voltage, Write Margin, Read Margin and also threshold voltage during read/write operation. We have analysed both read margin for read ability and write margin for SRAM write ability with the Static Noise Margin. Static Noise Margin affects both read margin and write margin. Both read margin and write margin depends on the pull up ratio and cell ratio respectively. The range of cell ratio should be 1 to 2.5 and also in case of pull up ratio, the W/L ratio of load transistor should be greater than the 3-4 times of the access transistor.

This project is based on the reliability of SRAM circuits and systems. We considered that the four major parameters (SNM, DRV, RM and WM) of SRAM cell. Finally, we can say that different types of analysis are directly proportional to the size of the transistor.

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