Designing A Re-Configurable Fractional Fourier Transform Architecture Using Systolic Array

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Abstract

FRFT (Fractional Fourier Transforms) algorithm, which has been derived from DFT, computes the angular domains within the time and frequency domains. This algorithm is increasingly used in the field of signal filtering, quantum mechanics and optical physics. In this paper we develop an efficient, systolic, re-configurable architecture for a particular type of FRFT called MA-CDFRFT (Multi Angle Centered Discrete FRFT). The benefit of this particular type of FRFT is that it computes all the signal components within equally spaced angles. Systolic architecture is used for this computation as it has certain advantages over the other forms like simplicity, regularity, concurrency and computation intensive The resultant product so developed should meet the challenges of today's market like marketable and cheap along with meeting customer demands. This calls for the architecture to be re-configurable. Re-configurable computer consist of a standard processor and an array of re-configurable hardware. The main processor would control the behavior of the re-configurable hardware. The re-configurable hardware would then be tailored to perform a specific task, such as image processing or pattern matching applications, as if it was built to perform this task exclusively.

Keywords: *MA-CDFRFT, Systolic Array, Up/down array, Re-configurable PE.*

1. Introduction

The DFT algorithm has been replaced by FFT algorithm by the signal processing researchers for its lower computational complexity. Also DCT and DWT algorithms are finding increasing importance in the field of signal compression. DFT had only one basic definition and a variety of algorithms have been devised for its fast computation. But when FRFT is analyzed in discrete domain, there are many definitions of discrete fractional Fourier transform (DFRFT) [3]. We first define Centered DFRFT (CDFRFT) and extend this definition to Multi-Angle CDFRFT (MA-CDFRFT). All through we shall use the definition given by [1]. Our proposed architecture can handle real time data and has reduced computational complexity using systolic up/down array in FFT computation. We then propose a re-configurable architecture for FRFT. The last of these steps corresponds to FFT implementation. Finally we construct a re-configurable PE, which will work for each stage. The various stages of the PE is generated by a set of signals from the control unit.

2. Related works

An architecture of FRFT has been proposed by Sinha et. al. [16] but that method is not suitable for real time data. Dick has proposed a method of computing DFT on FPGA based Systolic Arrays [8]. Dick also proposed a method for computing multi-dimensional DFT using Xilinx FPGA [17]. Cho et.al. discussed a implementation of DCT algorithm for parallel architecture[18]. A re-configurable architecture has been discussed by Acharya et. al.[19][20].

3. Computation of MA-CDFRFT

CDFRFT can be expressed [1] using Equation 1 as follows

$$\{A_{\alpha}\}_{kn} = \sum_{p=0}^{N-1} V_{kp} V_{np} e^{-jp\alpha} \quad (1)$$

Where V_{kp} is the k-th element of eigenvector p. Multiplying A_{α} by the signal element x[n] and rearranging, we obtain

$$X_\alpha[k] = \sum_{p=0}^{N-1} V_{kp} \sum_{n=0}^{N-1} x[n]\, V_{np} e^{-jp\alpha} \quad (3)$$

For a set of equally spaced values of a given by:

$$\alpha_r = 2\pi r/N \qquad r=0,1, \ldots ,N-1 \quad (4)$$

that correspond to the cases for which the trace of Aa becomes zero, we can rewrite the transform in terms of index r as

$$X_\alpha[k] = \sum_{p=0}^{N-1} V_{kp} \sum_{n=0}^{N-1} x[n]\, V_{np} e^{-j(2\pi/N)pr} \quad (5)$$

For the ease of computation we define $Z_k^+[p]$ as

$$Z_k^+[p] = \sum_{n=0}^{N-1} x[n]\, V_{np} \quad (6)$$

Again defining $Z_k[p]$ as

$$Z_k[p] = V_{kp} \sum_{n=0}^{N-1} x[n]\, V_{np} \quad (7)$$

we can see that the transform can be expressed as a DFT, that is

$$X_\alpha[k] = \sum_{p=0}^{N-1} Z_k[p]\, e^{-j(2\pi/N)pr} \quad (8)$$

where r=0,1,……,N-1 and k=0,1,……,N-1. Since Xk[r] contains all the CDFRFTs' corresponding to the discrete set of angles ar. [1] suggested that this matrix be called Multi-angle-CDFRFT or MA-CDFRFT.

4. Proposed FRFT Architecture

In the first step (Figure 1) the elements of the Eigen vector element Vnp are loaded into the processing elements [20].

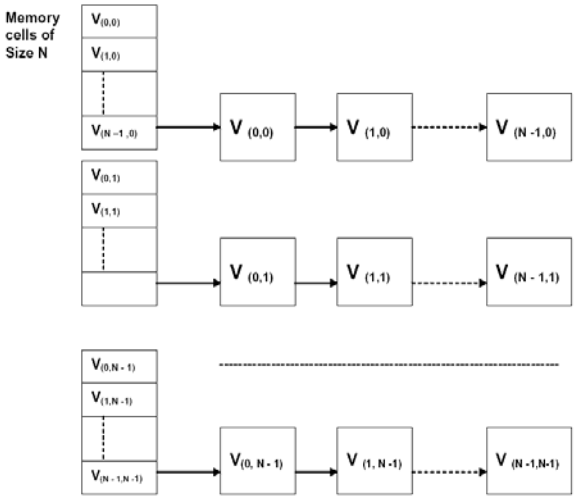

Fig 1. Loading of Constants V_{np}

In the second step (Figure 3) each of the signal elements are multiplied with the Eigen vector element Vnp. In the first cycle V_{00}, V_{10},…, V_{n0} is multiplied by x[0], x[1], ….., x[N-1] respectively. In the next cycle these multiplied values move to the second row whereas the first row multiplies the next set of signal elements with V_{11},…, V_{n1}. Finally in cycle N the value derived from each of the processing element are added at ∑ and the value $Z_k^+[0]$ is derived.

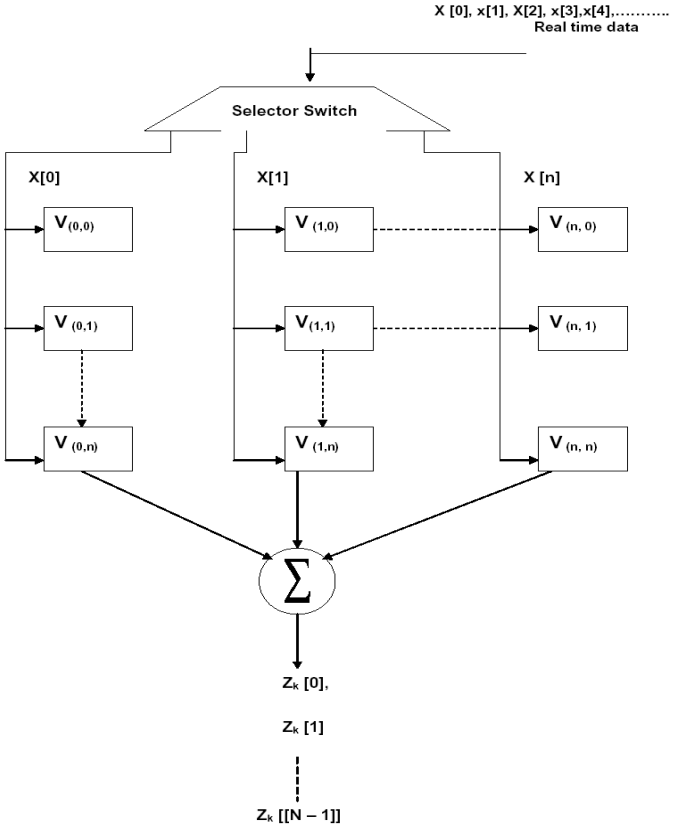

Fig 2. Multiplying each single element by V_{np} & taking the sum

We now discuss the third step (Figure 5) of FRFT architecture [20].. The elements derived at ∑ (the adder) of step 2 of FRFT are transferred systolically to the processing elements containing the elements containing V_{00}, V_{01}, … … , V_{N-10}. Thus the elements $Z_k[0]$, $Z_k[1]$,…..,$Z_k[N-1]$ are derived(Figure 5).

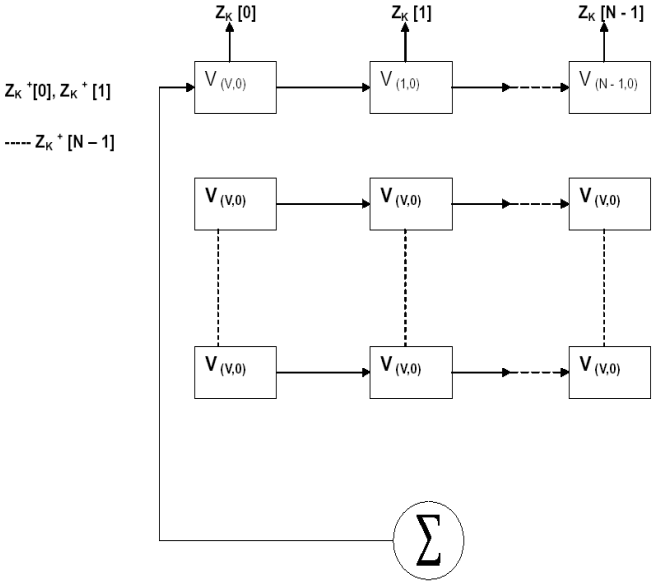

Fig 3. Calculation of $Z_k[P]$

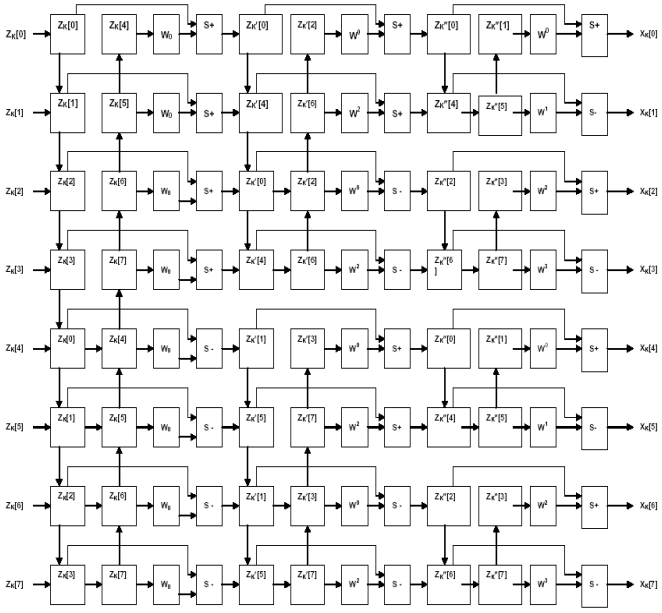

Fig 4: Detailed Working of the up/down array in FFT architecture

This element multiplied by the twiddle factor summed from 0 to N-1 gives the corresponding FRFT component for the rth plane. This computation can be done in a fast manner using FFT. We propose this computation be done using a UP/DOWN systolic array [19], which essentially consists of one upwards path for the bottom N/2, sets of input data and a downward path for the top N/2 sets of input data.

5. Computational Complexity of the Architecture

First we define Utilization Factor: Let there be N number of processing elements. In a particular cycle i, if N_i be the number of processing elements used (N_i<=N) then the utilization factor at cycle i is defined as

$$U_i = N_i/N$$

We divide the computation into the following stages:

In the first stage v_{np} is loaded in the systolic array. We assume there are N cells which stores V_{0p} to V_{N-1p} and T_1 is the transfer time of the signal element from the left to the right cell. Then the time needed to fill the two dimensional systolic array is NT_1. Here the utilization factor of the systolic array after NT_1 time is 100 percent. In the second stage computation of $\sum x[n]\, v_{np}$ is done. We assume that clock period of real addition is T_2 and clock period to switch between real to imaginary signal components the selector switch [20] is T_3 then the total time is:

$$N(N-1)/2*T_1 + T_2 \log_2 N + T_3.$$

The PE utilization is 50% in this stage.

In the third stage f $\sum v_{kp} \sum x[n]\, v_{np}$ is computed. Again we assume the time for real multiplication and real addition is T_4 and to configure the required connection is T_5. So the total time required in this stage is T_4+T_5. The PE utilization is 50% in this stage.

In the final step Computation of FFT components are done. As the size of the longest up/down is N/2 and the number of stages is $\log_2 N$ the total computation time is:

$$[1 + N/2 \text{ up/down}] \log_2(N)$$

1 unit of time is chosen for each addition. Here the PE utilization is 100% after $[1 + N/2 \text{ up/down}] \log_2(N)$ time unit.

The above information may be summarized as follows

Table 1: FRFT calculation of Time complexity of different stages

Step	***Time Required***	***Time Complexity***
1	NT_1	O (N)
2	$N (N-1)/2*T_1 + T_2 \log_2 N + T_3$	$O (N^2)$
3	T_4+T_5	O (1)
4	$[1 + N/2 \text{ up/down}] \log_2 (N)$	$O (N \log_2 N)$

6. Re-configurable FRFT Architecture

In our proposed architecture we propose a re-configurable processing element, which can be dynamically reconfigured for different stages of FRFT. The processing element is controlled by a control unit, which generates control signal to do the necessary reconfiguration. As the architecture is systolic, each processing element has two inputs H_{in} & V_{in} used for sending necessary reconfiguration signals and two outputs H_{out} & V_{out} [20].

The process of reconfiguration is discussed stepwise Firstly, eigen vector elements V_{np} is systolically transferred through H_{in} and the vector components is stored in the register R1 and R2. R3 will initially store the zero and R1 is bypassed to H_{out}. Secondly, the signal component V_{np} transferred through H_{in} is multiplied with the register value of R1 and then this value is added with the signal component X (n, p-1) transferred through V_{in} and stored to the register R3. Then the value is by passed through V_{out}. In the third stage the signal H_{in} is stored in the register R1. Then this valued is transferred to H_{out}. Next the value of the register R1 and R2 is multiplied and stored in the register R3. The output is the vector $Z_K[p]$. Finally, the value of the signal element H_{in} is stored to the register R2 and the value of the register R3 and R2 is multiplied and stored to the register R4. This finally yields the transform vector $X_\alpha[k]$

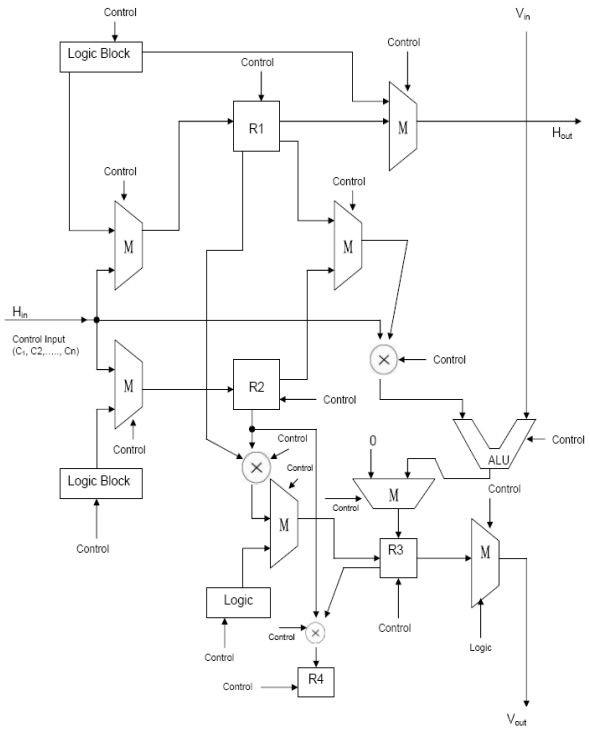

Fig 4: Reconfigurable Processing Element for computation of MA-CDFRFT

7. Conclusions

In this paper we discussed a re-configurable architecture that computes MA-CDFRFT transforms in four stages. The algorithm developed has a complexity of order ($N^2 \log N$). We discuss some other features that could make the architecture more versatile. Firstly the architecture could be made more Fault Tolerant so that a failed PE is disabled. The rest of the system continues to function as usual. Secondly since there is multiple PEs, there can be multiple simultaneous users of the system, each executing a different task. Thirdly we could use systolic rings to improve inter PE communication instead of systolic array. This architecture could be extended to computation of other image processing algorithms like DCT, DWT, FFT [15] and DFT. This could lead to the development of a generalized transform processor in which a single PE, upon the effect of a control signal, could compute various transforms.

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