

Designing of Efficient Adders by using a Novel Reversible SDNG gate

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Abstract

In recent years, reversible logic circuits are increasingly used in power minimization and having applications such as low power CMOS design, optical information processing, DNA computing, bioinformatics, quantum computing and nanotechnology. Under ideal conditions, reversible logic gates produce zero power dissipation. The main motivation behind the study of this technology is aimed at implementing reversible computing where they offer what is predicted to be the only potential way to improve the energy efficiency of computers beyond von Neumann-Landauer limit. Implementing the reversible logic has the advantages of reducing gate counts, garbage outputs as well as constant inputs. In this paper, a new 4*4 reversible logic gate SDNG is proposed. The SDNG gate can be used to implement all types of classical Boolean applications like XOR, XNOR, NAND, NOR, AND, OR, and NOT. It also can be used to design various adders efficiently. One of the prominent functionalities of the SDNG gate is that it can work singly as a full adder, or full subtractor, which is a versatile and widely used element in digital design. Thus, the proposed reversible full adder/subtractor contains only one gate. This paper also represents 4 bit Parallel adder circuit, 4 bit Parallel subtractor circuit, 2's Complement adder-subtractor circuit, Carry skip adder circuit, BCD adder circuit and carry skip BCD adder circuit which have been implemented by using this proposed SDNG reversible gate. Also SDNG gate and SDNG gate as a full adder and full subtractor has been simulated by XILINX and implemented in the SPARTAN - FPGA Kit.

Keywords: Nanotechnology, reversible logic gate, reversible full adder, reversible subtractor, reversible computing, quantum computing, BCD adder, ripple carry adder.

1. Introduction

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation. Researchers like Landauer have shown that for irreversible logic computations, each bit of information

lost, generates $kT \log 2$ joules of heat energy, where k is Boltzmann's constant and T is the absolute temperature at which computation is performed [1]. The primitive combinational logic circuits dissipate heat energy for every bit of information that is lost during the operation. Later Bennett, in 1973, showed that in order to avoid $kT \ln 2$ joules of energy dissipation in a circuit it must be built from reversible circuits [2]. Since the amount of energy dissipated in a system bears a direct relationship to the number of bits erased during computation. Bennett concluded that no energy would dissipate from a system if it would be able to return to its initial state from its final state regardless of what occurred in between [2]. According to Moore's law, the numbers of transistors will double every 18 months. As the Moore's law continues to hold, the processing power doubles every 18 months. The current irreversible technologies will dissipate considerable heat and can reduce the life of the circuit. Thus energy conservative devices are the need of the day. One of the main constraints in reversible logic is to minimize the number of reversible gates used and garbage output produced. In literature there are a number of existing reversible gate such as Fredkin gate [3,4,5], Toffoli gate [3,4] and Peres gate [6]. In this paper, a new reversible logic gate, SDNG is introduced. A versatile and widely used element, the full adder/subtractor circuit can be built with only one SDNG gate that has been demonstrated here.

2. Reversible Logic

2.1 Definitions of Reversible logic gate

Reversible Logic

The n -input and k -output Boolean function $f(x_1, x_2, x_3, \dots, x_n)$ (referred to as (n, k) function) is called reversible if:

- The number of outputs is equal to the number of inputs.
- Each input pattern maps to unique output patterns.

Reversible Logic Gate

Reversible Gates are circuits in which number of outputs is equal to the number of inputs and there is a one to one correspondence between the vector of inputs and outputs [7]. It not only helps us to determine the outputs from the inputs but also helps us to uniquely recover the inputs from the outputs.

Ancilla inputs/Constant inputs

This refers to the number of inputs that are to be maintaining constant at either 0 or 1 in order to synthesize the given logical function.

Garbage Outputs

Additional inputs or outputs can be added so as to make the number of inputs and outputs equal whenever needed. This also refers to the number of outputs which are not used in the synthesis of a given function. In certain cases these become mandatory to achieve reversibility. Garbage is the number of outputs added to make an n-input k-output function ((n; k) function) reversible.

Constant input

The words constant inputs denote the present value inputs that were added to an (n; k) function to make it reversible. The following simple formula shows the relation between the number of garbage outputs and constant inputs.

$$\text{Input} + \text{constant input} = \text{output} + \text{garbage. [8]}$$

Quantum Cost

Quantum cost refers to the cost of the circuit in terms of the cost of a primitive gate. It is calculated knowing the number of primitive reversible logic gates (1*1 or 2*2) required to realize the circuit. The quantum cost of a circuit is the minimum number of 2*2 unitary gates to represent the circuit keeping the output unchanged. The quantum cost of a 1*1 gate is 0 and that of any 2*2 gate is the same, which is 1 [9].

2.2 Reversible logic gate

Feynman gate

The Feynman gate is a 2*2 gate and is widely used for fan-out purposes. The inputs (A, B) and outputs (P=A, Q=A XOR B). It has quantum cost one [10].



Fig. 1a. Feynman gate

Toffoli gate

Toffoli gate is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=B, R=AB XOR C. It has quantum cost five[4].

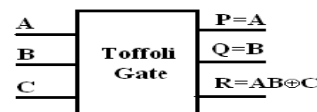


Fig. 1b. Toffoli gate

Fredkin gate

Fredkin gate is a 3*3 gate with inputs (A, B, C) and outputs P=A, Q=A'B+AC, R=AB+A'C. It has quantum cost five [3].

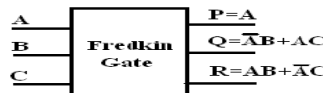


Fig. 1c. Fredkin gate

Peres gate

Peres gate is a 3*3 gate having inputs (A, B, C) and outputs P=A, Q=A XOR B, R=AB XOR C. It has quantum cost four [6].

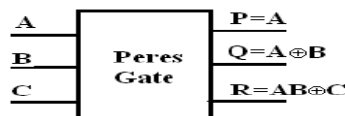


Fig. 1d. Peres gate

SCL gate

It is a 4*4 gate and its logic circuit is shown in the fig. [11].

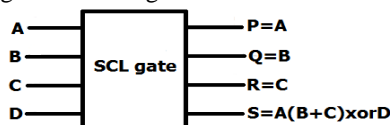


Fig. 1e. SCL gate

MKG gate

MKG gate is a 4*4 gate i.e. it comprises of four inputs and four outputs [12]

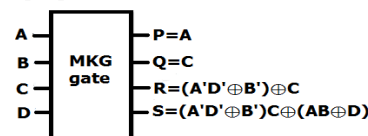


Fig. 1f. MKG gate

3. Proposed 4*4 SDNG Reversible Gate

This study proposes a new 4*4 reversible logic gate, SDNG shown in Fig. 2. Gate width of the proposed SDNG gate is four. In other words, SDNG is a 4-input, 4-output reversible logic gate. The SDNG gate can be represented as:

$$I_v = (A, B, C, D)$$

$$O_v = (P=A, Q=A XOR C, R = (A'D' XOR B') XOR C, S = (A'D' XOR B').C XOR (AB XOR D))$$

Where, I_v (A,B,C,D) and O_v (P,Q,R,S) are the input and output vectors, respectively and also one-to-one mapping function. The corresponding truth table of the SDNG gate is depicted in Table 1. It can be verified from the truth table that the input pattern corresponding to a particular output pattern can be uniquely determined.

$$P = \sum m(8, 9, 10, 11, 12, 13, 14, 15)$$

$$Q = \sum m(2, 3, 6, 7, 8, 9, 12, 13)$$

$$R = \sum m(1, 2, 4, 7, 8, 9, 14, 15)$$

$$S = \sum m(1, 5, 6, 7, 9, 10, 12, 14)$$

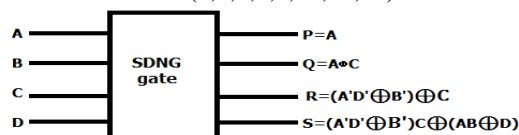


Fig.2. Proposed 4*4 reversible SDNG gate

Table1: Truth table for 4*4 SDNG reversible gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	1	1
0	0	1	0	0	1	1	0
0	0	1	1	0	1	0	0
0	1	0	0	0	0	1	0
0	1	0	1	0	0	0	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	1	1
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	0	0	1
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	1	1	0	0
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

4. Implementation of Classical Boolean Operations Using SDNG Gate

SDNG gate can be used for implementing arbitrary functions. It can implement all the Boolean functions shown in Fig. 3a to Fig. 3d. It can possible to get the copying function, NOT operation and NOR operation by using SDNG reversible gate shown in Fig. 3a. Fig. 3b. shows the implementation of the proposed SDNG reversible gate as copying and OR functions. Fig. 3c. represents the implementation of the proposed SDNG reversible gate as XNOR function. Fig. 3d. depicts the implementation of the proposed reversible gate as XOR and AND functions. Fig. 3e. represents the implementation of the proposed SDNG reversible gate as

copying, complementing and NAND operation.

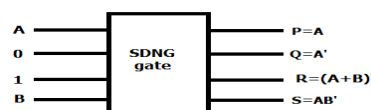


Fig.3a. SDNG gate as copying, NOT and NOR operations

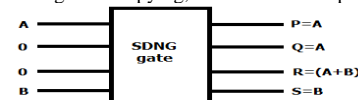


Fig.3b. SDNG gate as copying and OR operations

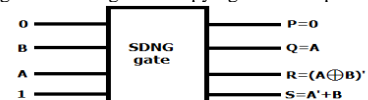


Fig.3c. SDNG gate as Null, Copying and XNOR operation

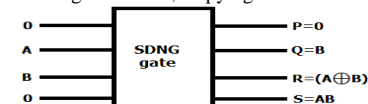


Fig.3d. SDNG gate as Null, Copying AND, XOR operation

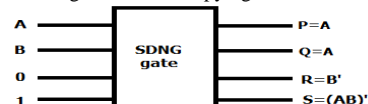


Fig.3e. SDNG gate as Copying, NOT and NAND operation

5. Literature Survey

A versatile arithmetic building element is the full adder. In the paper “A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems” [12], a full adder has been built using only one reversible MKG gate. It produces only two garbage outputs. It requires only one constant input and it needs only one clock cycle to perform the operations. Himanshu Thapliyal [13], “A New Reversible TSG gate and its application for designing efficient adders circuits” showed that the TSG gate is used to design optimized architectures of ripple carry and carry skip adders. The paper “Realisation of BCD adder using Reversible Logic” by X. Susan Christina, M. Sangeetha Justine, K. Rekha, U. Subha and R. Sumanthi [14] proposed novel designs of reversible BCD carry select and carry look-ahead adders. The simulation of these circuits has been done and they are ready to be used for designing large reversible systems which is the necessary requirement of quantum computers. The focus of Himanshu Thapliyal in the paper “Partial Reversible Gates(PRG) for Reversible BCD Arithmetic” [15] is the design of reversible BCD arithmetic units with minimal gates and garbage outputs. Thus, this paper proposes the novel concept of partial reversible gates which will satisfy the reversibility criteria not in all cases but for specific cases. In the paper, “Optimized reversible BCD adder using new reversible logic gates” by H.R.Bhagyalalxmi and M.K.Venkatesha [16], it is shown that the proposal is

highly optimized in terms of number of reversible logic gates, number of garbage outputs and the delay involved. Rangaraju H G, Venugopal U, Muralidhara K N, Raja K B [17] showed in the paper “Low Power Reversible Parallel Binary Adder/Subtractor”, that the reversible gates are used to implement full adder/subtractor and reversible eight-bit parallel binary adder/subtractor.

6. Conventional Irreversible Circuits

Half adder is a combinational arithmetic circuit that adds two numbers and produces a sum bit (S) and carry bit (C) as the output shown in fig 4. If A and B are the input bits, then sum bit (S) is the X-OR of A and B and the carry bit (C) will be the AND of A and B.



Fig.4. Half Adder

A Full Adder is a combinational circuit that performs the arithmetic sum of three input bits shown in fig 5. It consists of three inputs and two outputs. Three of the input variables can be defined as A, B, C_{in} and the two output variables can be defined as S, C_{out} . The two input variables A and B represents the two significant bits to be added. The third input C_{in} represents the carry bit. Two digits has to be used because the arithmetic sum of the three binary digits needs two digits. The two outputs represents S for sum and C_{out} for carry.

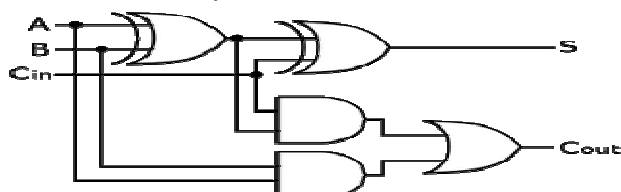


Fig. 5. Full Adder

In most logic circuits, addition of more than 1-bit is carried out. For example, modern computers and calculators use numbers ranging from 8 to 64-bits. The addition of multi bit numbers can be accomplished using several full-adders. The 4-bit adder using full-adder circuits is capable of adding two 4-bit numbers resulting in a 4-bit sum and a carry output as shown in Fig. 6. If all the bits of the augends and addend are fed into the adder circuits simultaneously, the addition in each position is taking place at the same time, and then the circuit is known as parallel adder shown in fig 6 which are faster.

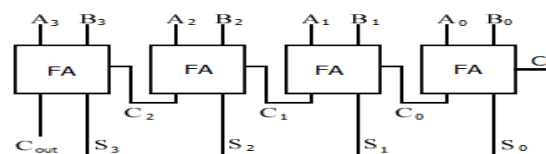


Fig. 6. Parallel Adder

The 2’s complement of a binary number can be obtained by adding 1 to its 1’s complement. The conventional 2’s complement Adder/Subtractor circuit is shown in fig 7, which can be controlled by the ADD’/SUB line. When ADD=0, the circuit performs as an Adder but when SUB=1 it acts as a Subtractor.

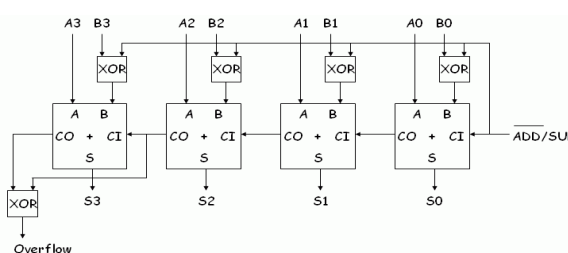


Fig. 7. 2’s complement adder/subtractor

A carry-skip adder (also known as a carry-bypass adder) is an adder implementation that improves on the delay of a ripple-carry adder shown in fig 8. The two addends are split in blocks of n bits. The output carry of each block is dependent on the input carry only if, for each of the n bits in the block, at least one addend has a 1 bit. A carry skip adder consists of a simple ripple carry-adder with a special speed up carry chain called a skip chain. This chain defines the distribution of ripple carry blocks, which compose the skip adder.

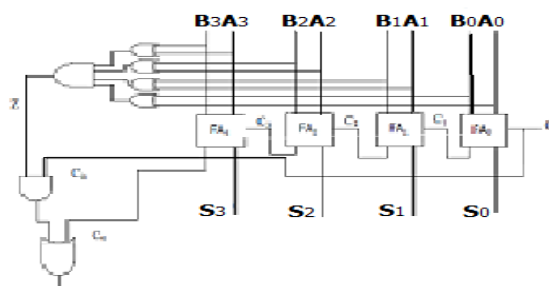


Fig. 8. Carry skip Adder

A BCD adder is a circuit that adds two BCD digits in parallel and produces a sum digit which is also in BCD shown in fig 9. A BCD adder must include the correction logic in its internal construction. A block diagram for the BCD adder is shown in Fig. 6. This adder has two-bit BCD inputs $A_3A_2A_1A_0$, $B_3B_2B_1B_0$ and a carry input (C_{in}). It also has a 4-bit sum output ($S_3S_2S_1S_0$) and a carry output (C_{out}). Here, the sum output is also in BCD form.

- A BCD adder circuit must be able to do the following:
- 1) Add two 4-bit BCD numbers using straight binary addition
 - 2) If the four-bit sum is equal or less than 9, the sum is in proper BCD form and no correction is needed.
 - 3) If the four-bit sum is greater than 9 or if a carry is generated from the sum, the sum is not in the BCD form.

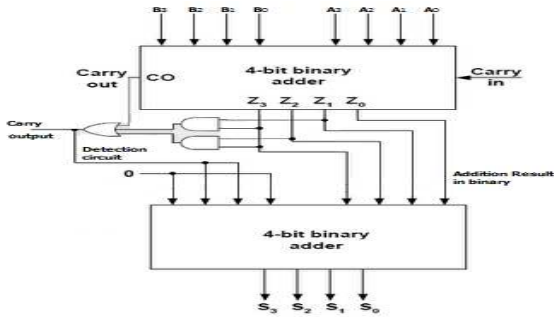


Fig. 9. BCD Adder

Then, the digit 6 (0110) should be added to the sum to produce the BCD results. The carry may be produced due to this addition and it is added to the next decimal position. Therefore, the condition for correction can be written as an expression as follows:

$$F=C_0+Z_3Z_2+Z_3Z_1$$

Where C_0 is the output carry, and the Z_3 is the 4th bit, Z_2 the bit 3 and similarly Z_1 bit 2.

The circuit is as shown in Fig. 10. It uses two four bit adders, carry skip logic circuit and a correction logic circuit. The carry skip BCD adder is faster than the above BCD adder as it skips the propagation of carry input if $Z=1$. The carry propagate input $Z=Z_0.Z_1.Z_2.Z_3$ is generated at the output of a 4-input AND gate where $Z_0=(A_0 \oplus B_0)$, $Z_1=(A_1 \oplus B_1)$, $Z_2=(A_2 \oplus B_2)$ and $Z_3=(A_3 \oplus B_3)$. When $Z=1$, the carry input C_{in} is propagated to reach C_{out} , otherwise it is skipped without propagating through the full adders. If $Z=0$, C_4 is propagated to C_{out} . Also whenever $C_{out}=1$, correction logic adds six to the sum to generate the correct BCD sum as per rules of BCD addition.

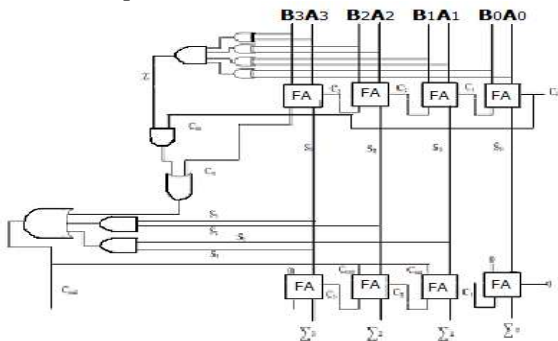


Fig. 10. Carry skip BCD Adder

7. Proposed Design Approaches Using SDNG gate

7.1 Design of Half Adder and Full Adder/ Half subtractor and full subtractor using SDNG gate

The binary full adder/subtractor is capable of handling one bit of each input along with a carry in/borrow in generated as a carry out/ borrow from addition of previous lower order bit position. Here half adder, Full Adder, Half subtractor and Full Subtractor has been implemented by using a single SDNG gate for each case shown in fig11a, fig 11b, fig 12a and fig 12b respectively. If two binary numbers each consisting of n bits are to be added or subtracted, then n numbers of binary full adders/subtractors are to be cascaded. A Parallel adder/subtractor is an interconnection of full adders/subtractors and the inputs are simultaneously applied. The carry/borrow generated at a stage is propagated to the next stage.

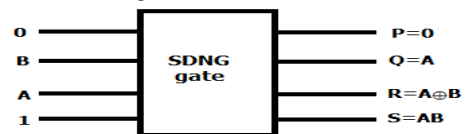


Fig. 11a. Reversible Half Adder using SDNG gate

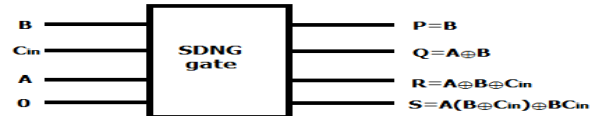


Fig. 11b. Reversible Full Adder using SDNG gate

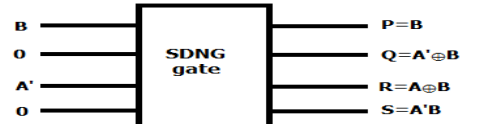


Fig. 12a. Reversible Half Subtractor using SDNG gate

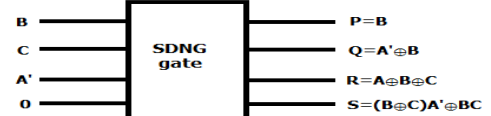


Fig. 12b. Reversible Full Subtractor using SDNG gate

7.2 Design of 4-bit parallel adder and parallel subtractor using SDNG gate

A 4 bit reversible parallel adder and subtractor is implemented using the reversible SDNG gate and shown in Fig. 13 and fig 14 respectively.

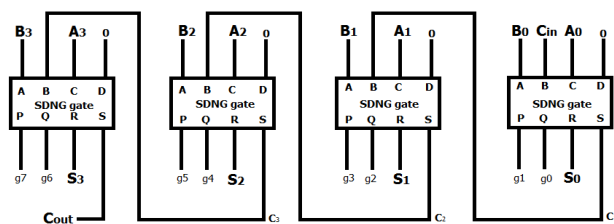


Fig. 13. 4-bit Parallel Adder

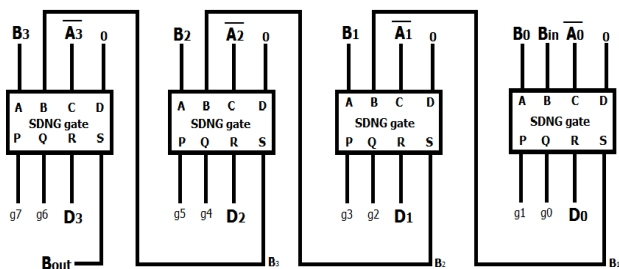


Fig. 14. 4-bit Parallel Subtractor

7.3 Design of 4-bit 2's complement adder – subtractor using SDNG gate

The 4-bit parallel binary adder/subtractor circuit shown in Fig. 15 performs the operations of both addition and subtraction depending upon the control line. A 4 bit 2's complement adder-subtractor circuit of reversible parallel adder/subtractor has been implemented here using the reversible SDNG gate as an full adder and XOR gates are replaced by reversible Feynman gate. When the control line $M=0$, the first number is given as been provided, the circuit acts as a parallel adder, thus adding two binary numbers of 4 bit each and produces a 4 bit sum and a carry out, as shown in Fig 13. If the control line $M=1$ the circuit acts as a parallel subtractor, thus subtracting two binary numbers of 4 bits each and produces a 4 bit difference and a borrow out, as shown in Fig. 14. The same design can be extended to n bits.

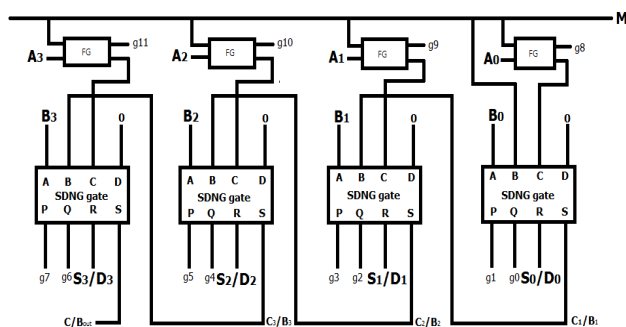


Fig. 15. 2's complement Adder/Subtractor

7.4 Design of Carry Skip Adder using SDNG gate

The carry skip block replaces the AND2-OR2 gate combination with a single Peres gate. Fig. 16 shows the block diagram of the carry skip adder block constructed with Peres gates and SDNG gates. The three Peres gates in the middle of Fig. 16 perform the AND4 operation generating the block propagate signal P . The single Peres gate in the left side of Fig. 16 performs the

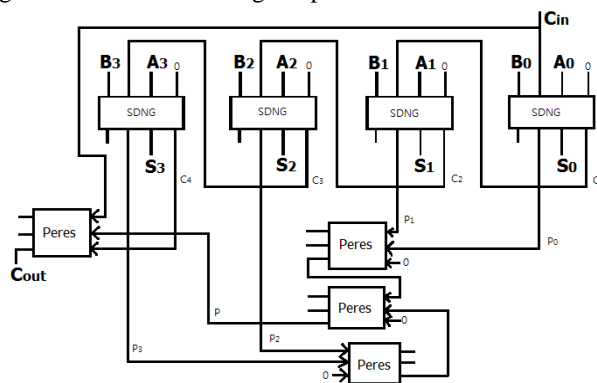


Fig. 16. Carry skip adder using SDNG and Peres gate

AND-OR function to create the carry skip logic and block carry out signal C_{out} . The Peres gate propagates signal the block's carry input to the next block if the block propagate signal P is one; otherwise the Peres gate propagates the most significant full adder carry C_4 to the next block.

7.5 Design of BCD Adder using SDNG gate

A one digit BCD adder adds two BCD numbers and produces the BCD sum after the required correction which is according to the rules for BCD addition. The BCD adder can be constructed using reversible gates. Fig 17 shows the 4 bit parallel adder constructed using SDNG gates. The proposed BCD adder circuit uses one such 4 bit parallel

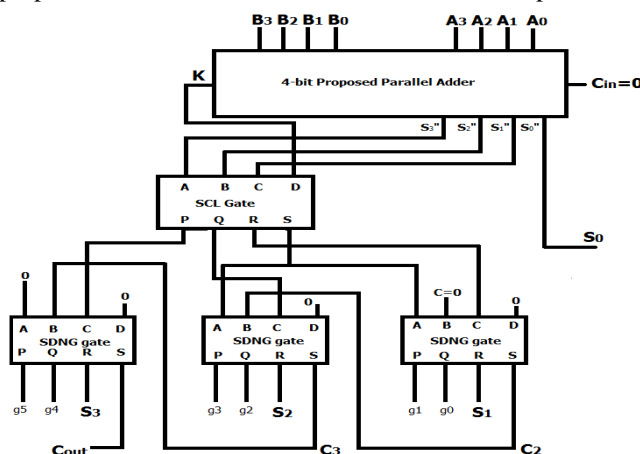


Fig. 17. BCD Adder using SDNG gate

and three full adders. The total number of garbage outputs generated from the reversible parallel adder is equal to eight. The overflow detection uses one SCL gate. This does not produce three garbage outputs. Also the second adder which should add six in order to correct and convert the sum to BCD sum need not be a 4-bit parallel adder but instead it can be constructed using three SDNG gates as full adders which is slightly different from the existing designs. [18-19].

7.6 Design of Carry skip BCD Adder using SDNG gate

Four DKFG reversible gates have been used as a full adder to add two four bits BCD numbers $A_3A_2A_1A_0$ and $B_3B_2B_1B_0$. For initial input carry C_{in} is used which will give C_4, S_3, S_2, S_1 and ΣS_0 . Three PERES gates have been used for getting $Z = Z_3Z_2Z_1Z_0$ where $Z_0 = (A_0 \oplus B_0)$, $Z_1 = (A_1 \oplus B_1)$, $Z_2 = (A_2 \oplus B_2)$ and $Z_3 = (A_3 \oplus B_3)$. An another PERES gate has been used to create $P = ZC_{in} + C_4$. Then the SCL gate has been used for six correction logic and from where the carry output $C_{out} = PS_3(S_2 + S_1)$ can be achieved. Another PERES gate has been used for adding S_1 and C_{out} . Finally ΣS_1 can be achieved and the generated carry is forwarded to next SDNG gate. Again the SDNG gate is used as a full adder to add the previous generated carry from the PERES gate, S_3 and C_{out} . And from this SDNG gate the C_{out} and ΣS_2 can be got and the generated carry is forwarded to the FG gate. Finally ΣS_3 can be achieved from FG gate. Lastly the corrected BCD can be drawn as $\Sigma S_3\Sigma S_2\Sigma S_1\Sigma S_0$.

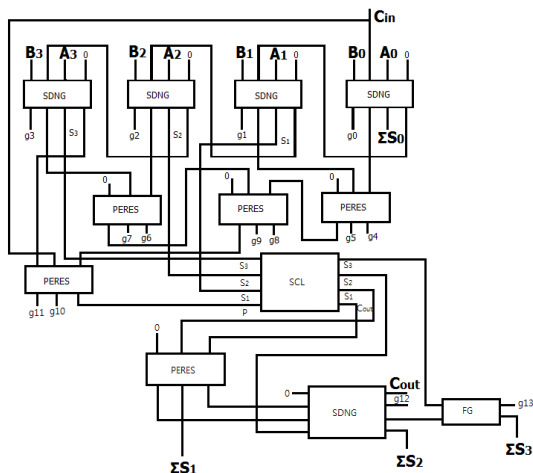


Fig. 18. Carry skip BCD adder using SDNG and Peres gate

8. Comparison

A comparison is made for all the designs of adder

subtractor circuit which is proposed in this paper by using reversible SDNG gate in terms of number of reversible gates, number of constant inputs and number of garbage outputs shown in Table 2.

Table 2: Comparison among the proposed designs

Name of proposed designs	No. of reversible gates	No. of constant inputs	No. of garbage output
Half adder	01	02	02
Half subtractor	01	02	02
Full adder	01	01	02
Full subtractor	01	01	02
4 bit Parallel Adder	04	04	08
4 bit Parallel Subtractor	04	04	08
2's complement Adder/subtractor	08	08	12
BCD Adder	08	10	14
Carry skip Adder	08	07	12
Carry skip BCD Adder	12	09	13

A comparison is also made for the proposed Full adder/subtractor circuit with the existing circuits in terms of different parameters which is shown in Table 3.

Table 3: Comparison for Full adder/subtractor

Full Adder/Subtractor	I. Different Parameters		
	No. of Garbage Output	No. of Constant Input	No. of Reversible gates
Paper(17) - Design I	05	03	08
Paper(17) - Design II	03	01	04
Paper(17) - Design III	03	01	04
MUX (Paper-20)	06	05	08
TR(Paper-20)	07	05	09
HYBRID(Paper-20)	05	03	08
Proposed Design	02	01	01

A comparison is also made for the proposed BCD adder circuit with the existing circuits in terms of different parameters which is shown in Table 4

Table 4: Comparison for BCD adder

BCD Adder	I. Different Parameters		
	No. of Garbage Output	No. of Constant Input	No. of Reversible gates
Paper(21)	22	17	14
Paper(22)	22	17	23
Proposed Design	14	10	8

A comparison is also made for the proposed Carry Skip BCD adder circuit with the existing circuits in terms of different parameters which is shown in Table 5

Table 5: Comparison for Carry Skip BCD adder

Carry skip BCD adder circuit	I. Different Parameters		
	No. of Garbage output	No. of Constant input	No. of Reversible gates
Paper(23)	27	15	15
Paper(7)	14	11	15
Using HNG gate	13	10	16
Paper(24)	14	11	15
Paper(19)	14	10	13
Proposed Design	13	9	12

9. Results and Discussions

Various types of adders have been implemented in this work using SDNG gate. This work also includes the simulation of the proposed SDNG gate and 1 bit adder and subtractor using the proposed gate. The simulated snapshot input/ output waveform of the proposed circuits is shown from Fig.19. to Fig 24. The schematics are also shown from fig 25 to fig 27. The simulation has been done by XILINX ISE 8.2 and also the implementation in the SPARTAN-3 FPGA Kit has been achieved.

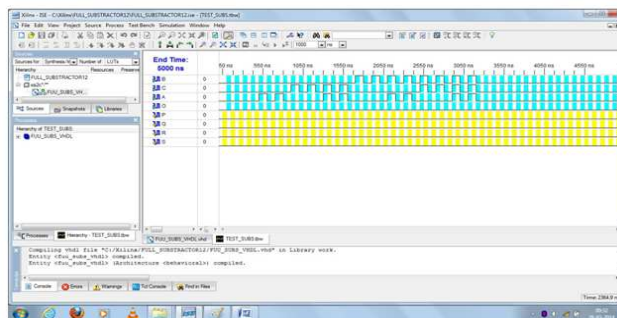


Fig. 21. Simulation result for input of 1 bit subtractor using SDNG gate

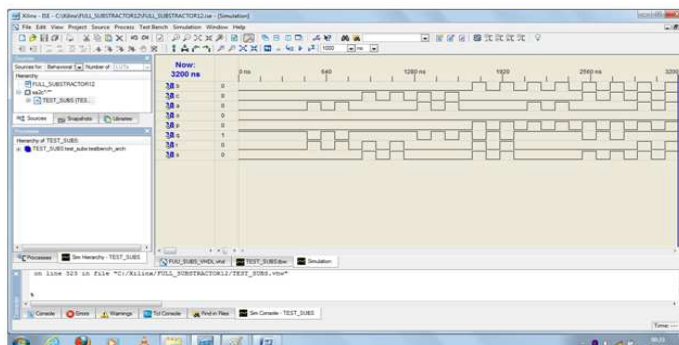


Fig. 22. Simulation result for output of 1 bit subtractor using SDNG gate

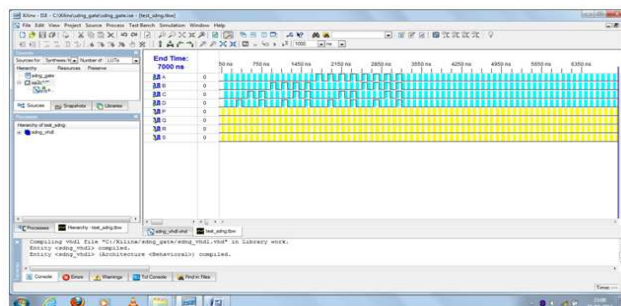


Fig. 19. Simulation result for SDNG gate input

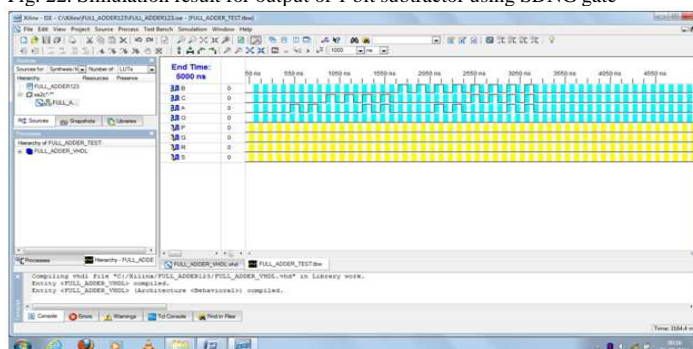


Fig. 23. Simulation result for input of 1 bit adder using SDNG gate

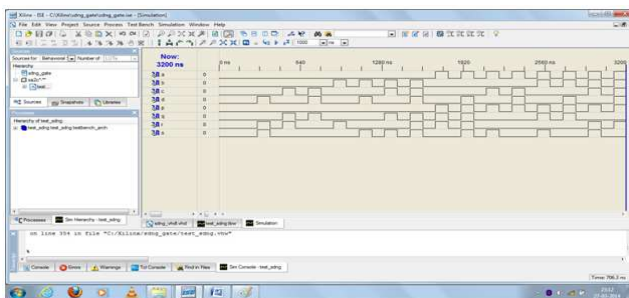


Fig. 20. Simulation result for SDNG gate output

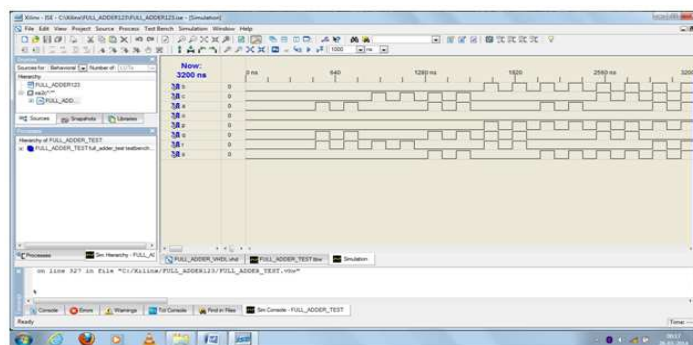


Fig. 24. Simulation result for output of 1 bit adder using SDNG gate

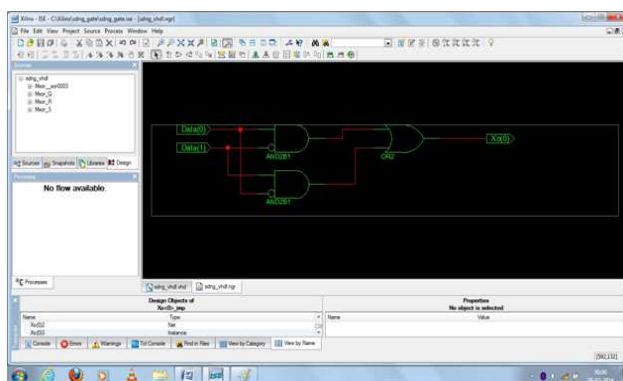


Fig. 25. Schematic for SDNG gate

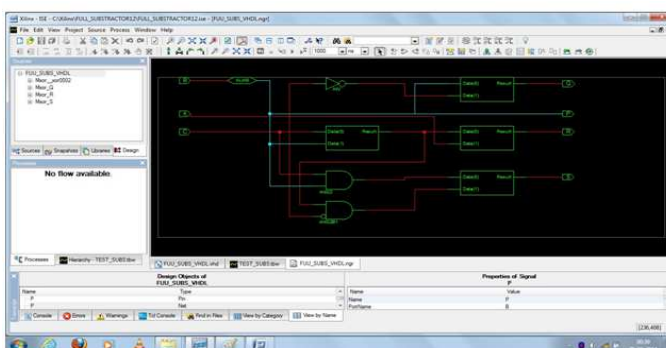


Fig. 26. Schematic for 1 bit subtractor using SDNG gate

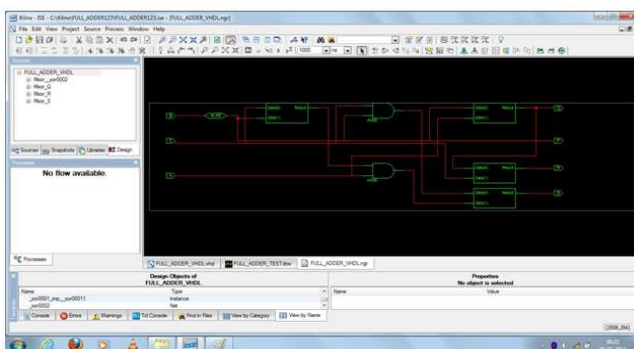


Fig. 27. Schematic for 1 bit adder using SDNG gate

10. Conclusions

This paper represents a new reversible SDNG gate. Various types of adders have been designed here using the proposed gate. In Table 2 a comparison is made within the proposed designs in terms of number of reversible gates, number of constant inputs and number of garbage outputs. The proposed designs seem more efficient in terms of different parameters with respect to the existing designs shown in the Table 3, Table 4 and Table 5. The simulation has been done by XILINX ISE 8.2 and also the implementation in the SPARTAN-3 FPGA Kit has been

achieved in this work. Using these adder subtractor circuits 8bit, 16 bit and N bits of different adders and subtractors can also be constructed in future. As adders are the primitive building blocks for designing ALU it plays a significant role in architecture designing. As a future work there is a vast application of these proposed design methods. Realization of these design methods using quantum dot cellular automata and also the testing of its functionality by simulation for checking the accuracy of these design methods can be treated as the probable future work.

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References

- [1] R. Landauer, - Irreversibility and Heat Generation in the Computational Process, IBM Journal of Research and Development, 5, pp. 183-191, 1961.
- [2] C. H. Bennett, - Logical Reversibility of Computation, IBM J. Research and Development, pp. 525-532, November 1973.
- [3] E. Fredkin, T Toffoli, "Conservative Logic", International Journal of Theor. Physics, 21(1982), pp. 219-253
- [4] T. Toffoli, "Reversible Computing", Tech memo MIT/LCS/TM-151, MIT Lab for Computer Science (1980)
- [5] Alberto LEPORATI, Claudie ZANDRON, Giancarlo MAURI, "Simulating the Fredkin Gate with Energy {Based P Systems}", Journal of Universal Computer Science, Vol. 10, Issue 5, pp. 600-619
- [6] Peres, "Reversible Logic and Quantum Computer", Physical review A, 32:3266-3276, 1985
- [7] Ashis Kumer Biswas, Md. Mahmudul Hasan, Moshaddek hasan, Ahsan Raja Chowdhury and Hafiz Md. Hasan Babu, - A Novel Approach to Design BCD Adder and Carry Skip BCD Adder. 21st International Conference on VLSI Design, 1063-9667/08 \$25.00 ©2008 IEEE DOI 10.1109/VLSI.2008.37
- [8] B.Raghu kanth, B.Murali Krishna, M. Sridhar, V.G Santhi Swaroop —A DISTINGUISH BETWEEN REVERSIBLE AND CONVENTIONAL LOGIC GATES, International Journal of Engineering Research and Applications (IJERA) ISSN: 2248-9622 www.ijera.com Vol. 2, Issue 2, Mar-Apr 2012, pp.148-151
- [9] J.Smoline and David P.DiVincenzo, — Five two-qubit gates are sufficient to implement the quantum fredkin gate, Physics Review A, vol. 53, no.4, pp. 2855-2856, 1996.
- [10] R. Feynman, "Quantum Mechanical Computers", Optical News. 1985, pp. 11-20
- [11] H. R. Bhagyalakshmi and M. K. Venkatesha, "Optimized reversible BCD adder using new reversible logic gates", Journal of Computing, Volume 2, Issue 2, February 2010, ISSN 2151-9617 arXiv:1002.3994v1.

- [12] Majid Haghparast, Keivan Navi, "A Novel Reversible Full Adder Circuit for Nanotechnology Based Systems", Journal of Applied Sciences 7 (24), pp.3995-4000, 2007
- [13] Himanshu Thapliyal, M.B. Srinivas, "A New Reversible TSG gate and its application for designing efficient adders circuits" Proceedings of the 10th Asia-Pacific Computer Systems Architecture Conference (ACSAC 05), Lecture Notes of Computer Science, Vol.3740, pp. 775-786. Springer-Verlag. Oct 2005.
- [14] X. Susan Christina, M. Sangeetha Justine, K. Rekha, U. Subha and R. Sumathi, "Realization of BCD adder using Reversible Logic", International Journal of Computer Theory and Engineering, Vol.2, pp. 1793-8201, 2010
- [15] Himanshu Thapliyal, Hamid R. Arabina, Rajnish Bajpai, Kamal K. Sharma, "Partial Reversible Gates(PRG) for Reversible BCD Arithmetic"
- [16] H.R.Bhagyalaxmi, M.K.Venkatesha, "Optimized reversible BCD adder using new reversible logic gates", Journal of Computing, Vol.2, pp.28-32, 2010
- [17] Rangaraju H G, Venugopal U, Muralidhara K N, Raja K B, "Low Power Reversible Parallel Binary Adder/Subtractor"
- [18] Himanshu Thapliyal, Saurabh Kotiyal, M.B Srinivas, "Novel BCD adders and their reversible logic implementation for IEEE 754r format", 19th International Conference on VLSI Design 2006.
- [19] H R Bhagyalakshmi, Optimized design of BCD adder and Carry skip BCD adder using reversible logic gates'International Journal on Computer Science and Engineering (IJCSE) ISSN: 0975-3397 Vol. 3, 4 Apr 2011,1439-1449.
- [20] V.Kamalakaran1, Shilpakala.V2, Ravi.H.N "DESIGN OF ADDER / SUBTRACTOR CIRCUITS BASED ON REVERSIBLE GATES" An ISO 3297: 2007 Certified Organization)Vol. 2, Issue 8, August 2013
- [21] Haghparast M. and K. Navi, 2008. A Novel reversible BCD adder for nanotechnology based systems. Am. J. Applied Sci., 5 (3): 282-288
- [22] Hafiz Md. Hasan Babu and A. R. Chowdhury, "Design of a Reversible Binary Coded Decimal Adder by Using Reversible 4-bit Parallel adder", VLSI Design 2005, pp-255-260, Kolkata, India, Jan 2005.
- [23] Thapliyal H., S. Kotiyal, M. B. Srinivas, 2006. Novel BCD adders and their reversible logic implementation for IEEE 754r format. Proceedings of the 19th International Conference on VLSI Design, 3-7 Jan2006.
- [24] K. Biswas, M. M. Hasan, A. R. Chowdhury, and H.M. Hasan Babu. Efficient approaches for designing reversible binary coded decimal adders. Microelectronics Journal.39(12) : 1693-1703, 08