Adaptive Jitter Reduction in All Digital Symbol Timing Recovery Loops

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Abstract

In this paper, an adaptive jitter reduction technique is presented to substantially mitigate the tracking jitter of symbol timing recovery loops (STRLs) in all digital receivers and, hence, enhance the overall performance of the loop. This has been achieved by a structure utilizing a notch filter in a cascade arrangement with the loop filter to suppress the undesired frequency components and preserve the DC value at the output of the loop filter, which represents the trial value of the symbol timing error. Also, to improve the acquisition time of the loop, a dynamic gain control feedback path is added in the structure. A bit error rate (BER) performance close to theoretical results in presence of additive white Gaussian noise (AWGN), a very fast acquisition time and a low computational complexity have been achieved.

Keywords: *Enhancement, Dynamic Gain Control, Bit Error Rate, Symbol Timing Synchronization, Acquisition Time.*

1. Introduction

Synchronization is an essential function in synchronous communication systems for the acquisition and tracking of the carrier and timing clock from the received signal when neither carrier nor clock is present. Symbol timing synchronization which consists of the detection and correction of the symbol timing errors must be performed at the all-digital receiver as well as carrier frequency and phase synchronization. Any reduction in the tracking jitter of the synchronizer can improve the overall performance of the system. Symbol timing recovery loops (STRLs) which are often based on the digital phase-locked loop (DPLL) are key components of modern communication systems, and have found a widespread application to lock onto the symbol timing component in the received signal, and, hence, attempt to adjust the timing of the received signal to its original location. Analysis, design and performance of DPLLs have been investigated extensively in the literature [1-3]. One of the problems in using any DPLL is the presence of undesired tracking jitter, which can deteriorate the overall performance of the system to an unacceptable level. In symbol timing synchronization, a low tracking jitter is a desirable feature to achieve a better bit error rate (BER) performance. One approach to reduce the excessive tracking jitter is to decrease the loop gain. The acquisition and tracking behavior of the loop is controlled by the loop gain factor. Higher values of loop gain factor result in a faster acquisition at expense of larger tracking jitter. On the other hand as loop gain factor decreases, the tracking jitter decreases but acquisition time increases, which is not desirable in applications such as those in low-Earth orbit (LEO) satellites [4] in which speed of acquisition is of prime importance. However, any increase of the gain will aggravate the jitter. Therefore, in practice, a compromise between the gain and jitter is found to establish a reasonable performance by choosing the loop gain factor to a level which results in an acceptable synchronization performance.

In [5] a technique for achieving fast settling and good stability in all digital phase-locked loops has been proposed, which utilizes self-monitoring to obtain the parameters necessary for feed-forward compensation. A DPLL architecture has been presented in [6] to adaptively optimize the tracking jitter using a jitter estimation block to achieve minimum jitter operation. The jitter reduction approach taken in [7] is based on making a modification to symbol timing error detection algorithms of [8] to reduce the level of jitter for M-PSK signals. In [9] a new dynamic gain modification algorithm has been proposed to enhance the speed of transient response and tracking behavior of DPLLs without changing the order of the loop. In this algorithm, the gain of the loop digital filter is made a function of the sampled value of the signal at every sampling instance. In [10] the effect of optical self-feedback on the timing jitter of a passively mode-locked (ML) laser is investigated. The influence of the delay time, feedback strength, and amplitude-phase coupling on the timing jitter shows that, with vanishing amplitude-phase coupling, greater timing jitter reduction can be achieved with long delay times and larger feedback strengths, when feedback is near resonance. A multiphase delay locked loop (DLL) that can calibrate the interphase error and guarantee the duty cycle of the output clock of the DLL is presented in [11]. A sense-amplifier-based phase detector is proposed for reducing dithering jitter. A DLL featuring

jitter reduction techniques for a noisy environment is described in [12]. It controls a loop response mode by monitoring the magnitude of input jitter caused by supply noise. This technique varies the probability of phase error tracking. It reduces the output jitter of the DLL due to a low effective variance of input phase error and a narrow effective loop bandwidth. A comparison between two methods of timing jitter calculation is presented in [13]. The integral method utilizes spectral area of the single side-band phase noise spectrum to calculate root mean square timing jitter. The results obtained show that a consistent timing jitter is found by the integral method.

A simple method for reducing the cycle-to-cycle jitter of clock signals is described in [14]. If the two clock signals have nearly the same average phase and independently-distributed phase noise, then the jitter at the output is less than that of the input signals. In [15] the random jitter and deterministic jitter analysis on the proposed polyphase filter (PPF)-based multiphase clock in frequency multiplier with reference to the benchmark jitter analysis of the multiphase clock counterpart using conventional DLL approach is presented. The analysis results have shown that the jitter performance of PPF-based design is better than that of DLL-based design. Ref [16] presents an adaptive-bandwidth phase-locked loop (PLL) that retains the optimal jitter performance over a wide frequency range via continuous background frequency calibration. The effective center frequency of the voltage-controlled oscillator (VCO) is calibrated by adjusting the feedforward division factor while a dual-PLL architecture hides the switching transients. The impairments caused by timing jitter are a significant limiting factor in the performance of very high data rate OFDM systems. In [17] it is shown that oversampling can reduce the noise caused by timing jitter. A new jitter reduction circuit is proposed for reducing the timing jitter in a serializer-deserializer (SERDES) in [18]. Instead of using elaborate hardware to calculate the jitter, the jittered signal's autocorrelation is used to remove the jitter. The motivation for this work was to provide a reduced jitter phase-locked loop, so that incorporating a built-in self-testing mechanism for PLL's and SERDES would be simplified. In [19], a standard-cell module to reduce jitter observed in the Free-Running Period Synthesizer is presented. This jitter is due to the required variation in period duration in order to obtain a precise frequency.

In this paper, an adaptive jitter reduction technique to mitigate the tracking jitter in symbol timing synchronizers employing DPLLs is proposed. This technique employs a structure incorporating a notch filter in a cascade arrangement with the loop filter and a dynamic gain control feedback path to modify the overall filtering performance of the STRL. A low tracking jitter is desirable to achieve a better BER performance. The details of improving the performance of STRL in terms of achieving an approximately jitter free tracking is presented in the sequel.

The organization of this paper is as follows. An overview of a system incorporating a typical STRL is presented in Section 2. The adaptive jitter reduction technique will be presented in Section 3, which will be followed by simulation results in Section 4. Finally, conclusions will be drawn in Section 5.

2. System Model

A typical STRL is often based on the DPLL, which consists of following essential components: a matched filter (MF), an interpolator, a TED, a loop filter, and a NCO [20]. The loop shown in Fig. 1 is an all-digital, non-data aided, asynchronous STRL where the MF and interpolator have been replaced by the polyphase filterbank [21]. The polyphase MF operates on samples of received signal arriving every T seconds. The TED operates on the polyphase MF output and updates its output once per symbol. This output represents the error associated with the current estimate of the time of the maximum eye opening, which is the best estimate of the symbol timing error. The trial value of the error is determined by smoothing the error estimates using a loop filter. The resulting signal at the output of the filter has information on the actual error estimated, acquisition time, and the tracking jitter. This signal is fed to a numerically controlled oscillator (NCO) which, in turn, together with a polyphase MF are used to adjust the symbol timing of the received signal to when it should be. The loop gain factor, β, which controls the speed of acquisition of the error, and the amount of the tracking jitter is designed based on the linearized model of the DPLL. It has been assumed that prior to symbol timing synchronization, the Doppler shift has been fully synchronized. In the next section, the adaptive jitter reduction technique is described.

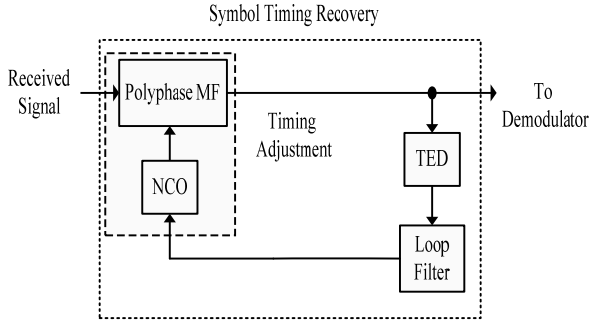

Fig. 1 STRL

The specifications of the baseband model of a system investigated are as follows

- Modulation: Quadrature phase shift keying (QPSK).
- TED: Gardner algorithm [8].
- Excess bandwidth of root raised cosine filters at the transmitter and receiver: 50%.
- Loop filter: A digital integrator.
- Channel: Additive white Gaussian noise (AWGN)

3. Adaptive Jitter Reduction

In the STRL shown in Fig. 1, by smoothing the timing estimate at the output of the loop filter and scaling the smoothed output by the loop gain factor, the trial timing error is obtained. During tracking, the trial value of the timing error consists of a desired DC component representing the actual timing error and an unwanted high frequency component known as jitter. The latter must ideally vanish. Jitter-induced errors can substantially deteriorate the BER performance. To improve the performance of STRL, the loop of Fig. 1 was enhanced as shown in Fig. 2 with an adaptive jitter reduction block whose main function is to single out the DC component with a fast acquisition time. This block consists of a second-order notch filter and a summing junction, as a jitter reduction block, in a cascade arrangement with the loop filter, and a differentiator with a summing junction and a multiplier in a feedback path. Ideally, all input frequency components except DC pass through the notch filter. By subtracting the output of the notch filter from its input, only DC will be present at the output of the jitter reduction block.

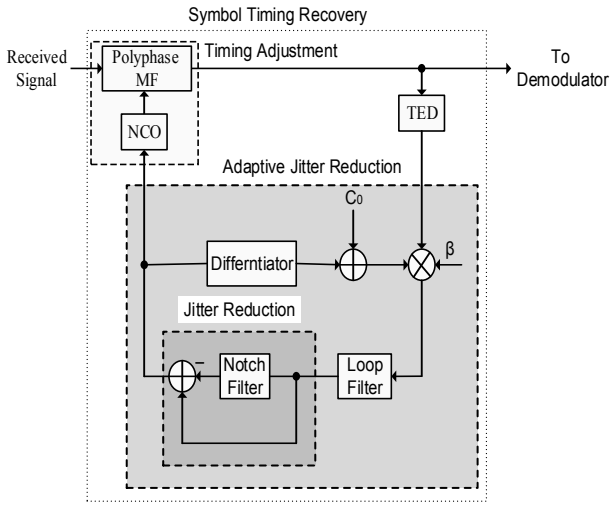

Fig. 2 Adaptive STRL

However, in practice, some frequency components about DC also appear at the output of the jitter reduction block. The feedback path plays a dynamic gain control role to improve the speed of the overall loop. Therefore, it is expected to see an approximately jitter free performance of the loop with a fast acquisition time.

3.1 Jitter Reduction

The transfer function of a second-order notch filter is [22]

$$H_{2N}(z) = K\frac{1-2\cos(\omega_0 T_s)z^{-1}+z^{-2}}{1-2r\cos(\omega_0 T_s)z^{-1}+r^2 z^{-2}} \quad (1)$$

where ω_0 is the notch frequency, r is the radius of the complex-conjugate pole pair located at the (normalized) frequency $\omega_0 Ts$, and K is a scaling factor. For the block to mitigate the tracking jitter, the notch frequency must be set to zero. Therefore,

$$H_{2N}(z) = K\frac{1-2z^{-1}+z^{-2}}{1-2rz^{-1}+r^2 z^{-2}} \quad (2)$$

which reduces to zero and $4K/(1+r)^2$ at $\omega Ts = 0$ and $\omega Ts = \pi$, respectively. Multiplication of Eq. (2) by $(1+r)^2/4K$ and subsequent subtraction from unity results in the following transfer function of the second-order jitter reduction block:

$$H_{2R}(z) = 1-\frac{(1+r)^2}{4}\frac{1-2z^{-1}+z^{-2}}{1-2rz^{-1}+r^2 z^{-2}} \quad (3)$$

which can be written as

$$H_{2R}(z) = \frac{\frac{(1-r)(r+3)}{4}\left[1+2\frac{1-r}{r+3}z^{-1}-\frac{3r+1}{r+3}z^{-2}\right]}{1-2rz^{-1}+r^2 z^{-2}} \quad (4)$$

whose magnitude response can be shown to be

$$\left|H_{2R}\left(e^{j\omega T_s}\right)\right| = \frac{(1-r)(r+3)}{4}\times \frac{\sqrt{2\left(1+\cos(\omega T_s)\right)\left(1+\left(\frac{3r+1}{r+3}\right)^2-2\frac{3r+1}{r+3}\cos(\omega T_s)\right)}}{1+r^2-2r\cos(\omega T_s)} \quad (5)$$

The response given by Eq. (5) has been plotted in Fig. 3. It is clearly seen that the input DC component is allowed to pass unattenuated while high frequency components are attenuated.

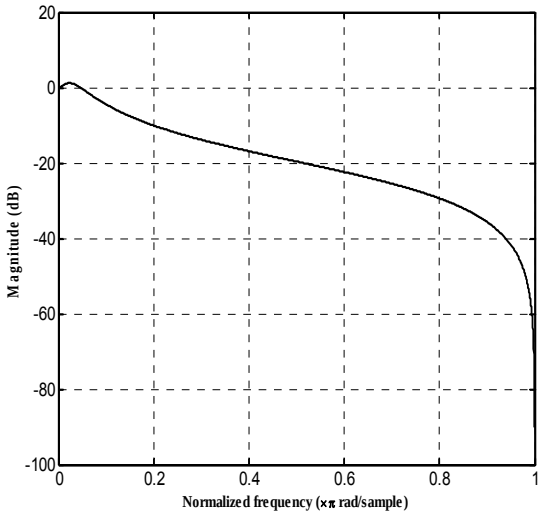

Fig. 3 Magnitude response of second-order jitter reduction block

Simulations in Section 4 confirm that blocks with such responses substantially mitigate the tracking jitter.

3.2 Dynamic Gain Control

The purpose of using the dynamic gain control feedback path within the adaptive jitter reduction block of STR loop in Fig. 2 is to dynamically change the loop gain factor; during acquisition the gain is high to increase the speed of the loop, while during tracking the gain is reduced to minimize the tracking jitter.

The difference equation between the input, $\tilde{\tau}[k]$, and output, $d[k]$, of the differentiator is expressed by

$$d[k] = \tilde{\tau}[k] - \tilde{\tau}[k-1] \tag{6}$$

where k is symbol number. The input, $\tilde{\tau}[k]$, also represents the trial value of the timing error. As the output of the differentiator is zero initially at $k = 0$ and ideally zero during tracking, a constant C_0 representing the initial gain tracking and tracking or steady-state gain of the STR loop is added. To minimize the tracking jitter, C_0 is taken as a small value. Therefore, the output of the summing junction becomes

$$g[k] = \beta(d[k] + C_0) \tag{7}$$

Where the scaling factor, β, represents the loop gain factor. Suitable values of C_0 and β are chosen by trial and error for different STR loops. Assuming the loop filter is a simple integrator, its output is

$$\tilde{\tau}[k] = \tilde{\tau}[k-1] + g[k]\hat{\tau}[k] \tag{8}$$

Where $\hat{\tau}[k]$ is the estimate of the timing error determined by the TED. Substituting Eq. (7) in Eq. (8) for $g[k]$ results in

$$\tilde{\tau}[k] = \tilde{\tau}[k-1] + \left[\beta(\tilde{\tau}[k] - \tilde{\tau}[k-1] + C_0)\right]\hat{\tau}[k] \tag{9}$$

In the presence of AWGN

$$\tilde{\tau}[k] = \tilde{\tau}[k-1] + \left[\beta(\tilde{\tau}[k] - \tilde{\tau}[k-1] + C_0)\right](\hat{\tau}[k] + w[k]) \tag{10}$$

where $w[k]$ is the AWGN sample. During tracking, $\tilde{\tau}[k]$ and $\tilde{\tau}[k-1]$ are practically close, and hence $\tilde{\tau}[k] - \tilde{\tau}[k-1]$ can be ignored. Therefore, Eq. (10) can be written as

$$\tilde{\tau}[k] \approx \tilde{\tau}[k-1] + \beta C_0(\hat{\tau}[k] + w[k]) \tag{11}$$

Since C_0 is chosen to be small during tracking, the unwanted components in Eq. (11), that is $\hat{\tau}[k]$ and $w[k]$, become small which is the prime motivation behind the jitter mitigation technique developed. There is no analytical expression relating β to C_0. In general, β must be large enough to guarantee a fast acquisition of the error without destabilizing the loop. Also, C_0 must be small enough to guarantee a low tracking jitter without the acquisition taking excessively long time.

3.3 Jitter Variance

The noise variance of the loop is given by [26]

$$\sigma^2 = \int_{-\frac{1}{2T}}^{\frac{1}{2T}} S_n(f)\left|H(f)\right|^2 df \tag{12}$$

Where $S_n(f)$ is the power spectral density of $n(kT)$, T is symbol period and $H(f)$ is the right-hand side of $H(z)$ for $z = \exp(j2\pi fT)$; $H(z)$ is transfer function of timing error output to $n(kT)$ input.

In some practical cases $S_n(f)$ is nearly flat over the noise equivalent bandwidth of the loop around the origin, where $H(f)$ takes significant values and Eq. (12) becomes

$$\sigma^2 = S_n(0) \int_{-\frac{1}{2T}}^{\frac{1}{2T}} |H(f)|^2 df \quad (13)$$

In the absence of AWGN, the only source of noise in the loop is due to self-noise of the timing error detector known as jitter. As a result, the source of the noise, $n(kT)$, can be represented at the output of the available TED in the tracking loop. So, frequency domain model of the symbol timing recovery loop at the presence of only self-noise can be shown as Fig. 4. In this figure, the loop transfer function required to compute jitter variance in Eq. (13), assuming $F(z)=1$ is given by

$$H(z) = \frac{\tau_e(z)}{N(z)} = \frac{-\beta K_0}{z - 1 + \beta K_0 K_p} \quad (14)$$

Where $N(z)$ is the Z transform of the noise, $n(kT)$, in the z-domain. By substituting $z = \exp(j2\pi fT)$ in Eq. (14),

$$H(f) = H(z)\big|_{z=e^{j2\pi fT}} = \frac{-\beta K_0}{e^{j2\pi fT} - 1 + \beta K_0 K_p} \quad (15)$$

And by substituting Eq. (15) in Eq. (13), and performing some simplifications, the jitter variance is found as

$$\sigma^2 = \frac{S_n(0)\beta K_0}{K_p(2 - \beta K_0 K_p)T} \quad (16)$$

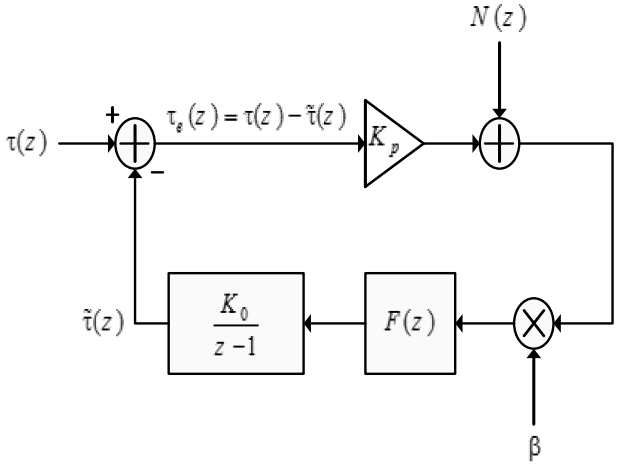

Fig. 4 Frequency domain model of the STRL at the presence of noise

But with the transfer function of the second order jitter reduction block, i.e. $F(z) = H_{2R}(z)$, the loop filter transfer function can be written as

$$H_2(z) = \frac{\tau_e(z)}{N(z)} = \frac{-\beta K_0 H_{2R}(z)}{z - 1 + \beta K_0 K_p H_{2R}(z)} \quad (17)$$

Using Eq. (4) it can be found that

$$H_2(z) = \frac{-\beta K_0 \frac{1-r}{4} \frac{(r+3)z^2 + 2(1-r)z - (3r+1)}{z^2 - 2rz + r^2}}{z - 1 + \beta K_0 K_p \frac{1-r}{4} \frac{(r+3)z^2 + 2(1-r)z - (3r+1)}{z^2 - 2rz + r^2}} \quad (18)$$

$$= \frac{-\beta K_0 \frac{1-r}{4}\left((r+3)z^2 + 2(1-r)z - (3r+1)\right)}{\left\{\begin{array}{l} z^3 - \left(2r + 1 - \beta K_0 K_p \frac{1-r}{4}(r+3)\right)z^2 + \\ \left(r^2 + 2r + \beta K_0 K_p \frac{(1-r)^2}{2}\right)z - r^2 \\ -\beta K_0 K_p \frac{1-r}{4}(3r+1) \end{array}\right\}}$$

By substituting $z = \exp(j2\pi fT)$ in Eq. (18), frequency response can be determined as

$$H_2(f) = H_2(z)\big|_{z=e^{j2\pi fT}}$$

$$= \frac{-\beta K_0 \frac{1-r}{4}\left((r+3)e^{j4\pi fT} + 2(1-r)e^{j2\pi fT} - (3r+1)\right)}{\left\{\begin{array}{l} e^{j6\pi fT} - \left(2r + 1 - \beta K_0 K_p \frac{1-r}{4}(r+3)\right)e^{j4\pi fT} + \\ \left(r^2 + 2r + \beta K_0 K_p \frac{(1-r)^2}{2}\right)e^{j2\pi fT} - r^2 \\ -\beta K_0 K_p \frac{1-r}{4}(3r+1) \end{array}\right\}} \quad (19)$$

By substituting Eq. (19) in Eq. (13), it is possible to compute the loop jitter variance with the second order jitter reduction block. In order to do that, from Eq. (13), the loop jitter variance with the second order jitter reduction block can be written as

$$\sigma_2^2 = S_n(0) \int_{-\frac{1}{2T}}^{\frac{1}{2T}} |H_2(f)|^2 df \quad (20)$$

To compute the amount of reduction in the loop jitter, with and without the jitter reduction block in the tracking loop, the ratio of the jitter variances can be written in two cases from Eqs. (16) and (20) as

$$\frac{\sigma_2^2}{\sigma^2} = \frac{\dfrac{S_n(0)\int_{-\frac{1}{2T}}^{\frac{1}{2T}} |H_2(f)|^2 df}{\dfrac{S_n(0)\beta K_0}{K_p(2-\beta K_0 K_p)T}}}{} = \frac{K_p(2-\beta K_0 K_p)T}{\beta K_0} \int_{-\frac{1}{2T}}^{\frac{1}{2T}} |H_2(f)|^2 df \quad (21)$$

By substituting Eq. (19) in Eq. (21), it is possible to compute the ratio of the jitter variances and as a result, the amount of reduction in the loop noise, with and without the jitter reduction block in the tracking loop, is determined. Under simulation conditions in the next section, from Eq. (21), the reduction in the loop jitter variance is about 37.5 dB which is compatible with the simulation results.

4. Simulation Results

A QPSK modem was simulated and the technique described was incorporated in the modem which was using the Gardner timing error detection algorithm. To test the performance of the system, the step simulation was set with a timing offset of $\tau = 4T_s = 0.25T$. The received data samples are processed by the polyphase MF filterbank with M = 16 stages. The loop gain factor was purposefully set to a high value to achieve a fast acquisition. Under such conditions, the results shown in Fig. 5 were obtained. The loop is trying to acquire the symbol timing error. However, it is not clear when the error has been acquired. Also, the loop is trying to track the timing error about the stable point. However, the tracking jitter present in the loop is noticeable.

Simulation of the adaptive loop using a second-order jitter reduction block with $r = 0.9$ at $\omega_0 Ts = 0$, and $\beta = 2.1$ was carried out under the same conditions that the modem with the original loop was simulated. The result shown in Fig. 6 was obtained. Unlike the original loop, the adaptive STRL has clearly acquired the error and after the acquisition time, the tracking jitter has been substantively mitigated. By computer evaluation it was found that the ratio of the jitter variances, with and without the adaptive jitter reduction block in the tracking loop, was -37.4 dB and as a result, the amount of reduction in the loop jitter is 37.4 dB which is approximately the same as the computed result from Eq. (21) under the simulation conditions. A much mitigated tracking jitter is the salient feature of the proposed enhancement. In order to emphasize the fast acquisition, the results in Fig. 6 have been shown over the first 110 symbols in Fig. 7. The acquisition time is about 55 symbols. Such a fast acquisition time is an attractive feature in applications such as those for a low earth orbit (LEO) satellites [4].

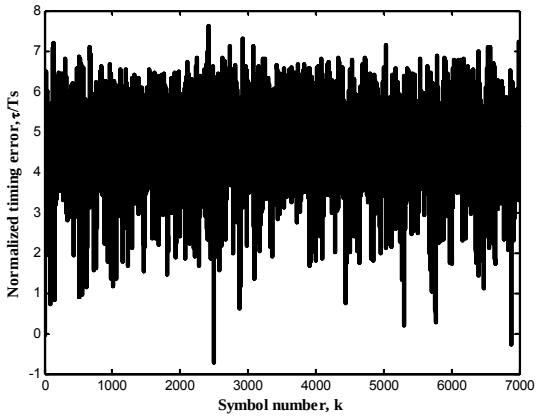

Fig. 5 Tracking performance before enhancement.

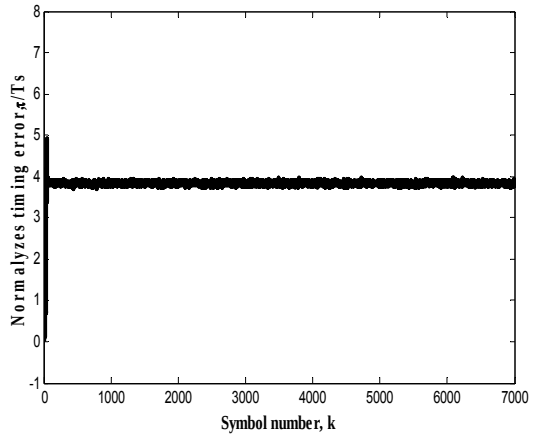

Fig. 6 Tracking performance after enhancement.

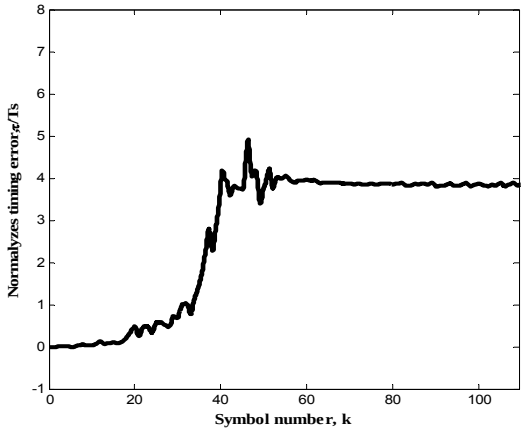

Fig. 7 Tracking performance after enhancement over the first 110 symbols

The Monte Carlo BER counting simulation performance of the original and adaptive STRLs when the received signal was plagued with AWGN are shown in Fig. 8. The total number of bits observed of %98 confidence was $M = 10^{N+2}$ for the theoretical BER of $p = 10^{-N}$ at any $Eb / N0$ [23].

BER performance before and after enhancement.

The theoretical BER results were plotted using $p = 0.5erfc(\sqrt{E_b / N_0})$, where $erfc(x)$ is the complementary error function of x, and $Eb / N0$ is the ratio of energy per bit to noise spectral density [24]. The BER performance of the original STRL is not acceptable at all. Excessive tracking jitter is the sole contributor to this poor performance. The simulation results of the original STRL enhanced with the adaptive jitter reduction block are also shown in Fig. 8 with signal-to-noise ratios (SNR) ranging from 0 to 10 dB. The BER results of the adaptive STRL, except at SNR = 0 dB, closely follow the theoretical performance, which is of great importance. A low tracking jitter has a major role in the resulting superior BER performance, which is close to theory. Also, the simulation results have been tabulated in Table 1, in which BERT, and BERE represent the theoretical BER, BER performance obtained with the second-order adaptive jitter reduction block, respectively. As is observed from the results, the BER performance obtained by using a second-order adaptive jitter reduction block, except at SNR = 0 dB, is marginal compared to the theoretical BER.

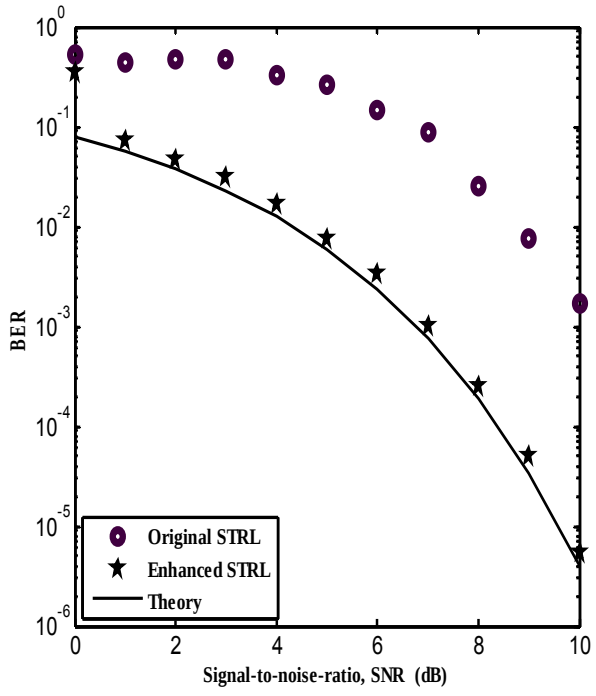

Fig. 8 BER performance before and after enhancement.

Table 1: BER Results of STRL with Second-Order Jitter Reduction Block

***SNR* (dB)**	***Theoretical BER* (BER_T)**	***Enhanced BER* (BER_E)**	$\lvert BER_E - BER_T \rvert$	$\left\lvert 1 - \frac{BER_E}{BER_T} \right\rvert$
0	0.0786496	0.3512841	0.2726345	3.4664448
1	0.0562820	0.0736456	0.0173636	0.3085107
2	0.0375061	0.0464938	0.0089877	0.2396330
3	0.0228784	0.0311356	0.0082572	0.3609169
4	0.0125008	0.0167745	0.0042737	0.3418741
5	0.0059539	0.0076011	0.0016472	0.2766590
6	0.0023883	0.0033510	0.0009627	0.4030901
7	7.727E-4	1.035E-3	0.0002623	0.3394590
8	1.909E-4	2.550E-4	0.0002459	0.3357779
9	3.36272E-5	5.09E-5	0.0000173	0.5136556
10	3.9E-6	5.5E-6	0.0000016	0.4102564

The implementation of adaptive jitter reduction block given in Eq. (4) is based on direct form II transposed structure [25]. The resulting number of delay elements, scaling factors, adders and multiplier is 3, 5, 5 and 1, respectively. It is clear that the computational complexity of adaptive jitter reduction block is low. This implies that it takes adaptive jitter reduction block less time to determine the output signal, which is of importance in fast applications. Such a low complexity is a highly desirable feature in hardware implementation. Therefore, a low computational complexity is another feature of the proposed technique.

The adaptive technique described is general, and can be applied to STRLs incorporating other TEDs. The aforementioned simulations were repeated with other symbol timing error detection algorithms such as the decision-directed maximum likelihood (ML) algorithm, and the data transition tracking loop (DTTL) algorithm [20]. Furthermore, the QPSK modulation scheme was changed to binary phase shift keying (BPSK), offset quadrature phase shift keying (OQPSK), and π/4-shifted differentially encoded quadrature phase shift keying (π/4-DQPSK) modulation schemes and simulations were repeated. The tracking and BER results obtained were consistently better when the proposed adaptive jitter reduction method was used.

5. Conclusions

In this paper, a new unified adaptive jitter reduction technique was presented to make the tracking performance of symbol timing recovery loops approximately jitter free. In light of the research carried out, a substantial improvement was made to the BER performance. The

achieved BER performance is close to the theoretical results. A low computational complexity, a fast acquisition time, and an operation independent of the modulation and error detection schemes are other features of the proposed technique.

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