

# TLM Platform Based on SystemC for Hybrid MSR Topology

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## Abstract

The Network-on-Chip (NoC) Architectures have been proposed as a revolutionary methodology to the communication of multi-core embedded processor in a chip. Interconnection topology plays an important role in communication locality of future CMPs. We suggest extracting the locality communication of sub tasks of applications. Indeed it is essential to provide a suitable NoC topology that exploits the locality of communication resource fully.

Due to the tradeoff between the performance and area constraint in on-chip network designs, we have developed in this paper a transactional level model NoC router of hybrid Mesh-Star-Ring. The new hybrid topology called Hybrid Locally Mesh Globally Star-Ring (HLMGSR) use the Star-Ring and mesh graphs as the basic building blocks. The experimental results show that for a network size equal to 128, the proposed hierarchical topology HLMGSR provides an area increase of 7% over the mesh. For a network size which is greater than or equal to 64 nodes, the lowest average latency is provided by the proposed hybrid topology for different injection rates. For a network size greater or equal to 64 nodes with the uniform traffic pattern with a lower injection rate, the results show that the HLMGSR provides the highest throughput.

**Keywords:** Network on chip, Hybrid NoC, Locality of Communication, TLM 2.0.

## 1. Introduction

System-on-Chip (SoC) provides single chip solutions in many applications require single or large chip implementations. To provide more computing power, designing multiprocessor system on chips (MPSoC) [1] can be used. MPSoC requires high-speed communication between processors which dependent on the fast and flexible interconnect network. Network-on-Chip (NoC) has been proposed as a promising approach for future multi-core systems, to overcome the problems of complexity and scalability of inter communication platform of SoCs composed by hundreds of cores. The interconnection topology acts an important role in communication locality inside chip multiprocessors. Many network architecture interconnections that are based on different standard topologies have been studied recently for SoC such as 2D Mesh [2], Torus [3], Fat-Tree (FT) [4], Ring [5], Butterfly-Fat Tree (BFT) [6], Spidergon [7],

Octagon [8]. These architectures are based on parallel concepts and distributed systems for interconnecting resources in a structured and scalable manner for ease of implementation.

The 2D-Mesh topology [3] is a popular topology used for NoC interconnects because of the regularity, the low complexity, and planer 2D layout properties. However, the large network diameter, suffers from large hop count that can increase the communication latency packets. The ring topology is characterized by the simplicity of its structure, lower average latency and high bandwidth. The ring topology has larger hop count with larger network diameter. However, the scalability of the ring topology can be limited [9].

The high performance parallel processing domain therefore admits very high dimensional and complex topologies that can greatly reduce its communication costs and improve its performance. Indeed, high-dimensional hyper-cubes are popular due to their ability to easily embed other problems [10].

The Star-Ring NoC topology [11] is a mixture of Ring and star topology. It was developed to fulfill the demands for the communication structure in the area of high performance computing. Therefore, it features a high throughput and a low latency.

Many architectures based on tiled exist ranging from Chip Multi-Processors (CMPs) to arrays of programmable logic or even to heterogeneous arrays that include custom-IP blocks.

Future massively parallel CMPs, will execute applications with enormous amounts of parallelism. We can have applications with significant amount of parallelism, or locality of communication, or both.

The mapping algorithm must also favor the locality of communication minimizing critical paths and congestion by using many sub-networks for local communication and one network for global communication. An application mapped on Network on chip based on such hybrid topology provides much higher bandwidth and lower-latency communication channels available between cores on chip. To further optimize NoC performance, it is expected that a combination of the benefits of different well established methodologies as such as a mesh, star,

ring, bus and point-to-point topology can provide benefits of both.

In this paper, we propose a new hybrid topology that can be personalized by the combination of the benefits of the 2D-Mesh, STAR and RING architectures MSR.

Our objective is to design a hybrid locally Mesh globally Star-Ring (HLMGSR).

The transaction level modeling methodologies has been proposed as a way to tackle firstly the HW/SW co-design problems and secondly the early architecture analysis [12]. To study the proposed topology in detail, we have developed a transaction level model of communication components of NoC such as link, routers which is implemented in SystemC TLM2.0. By integrating functions to calculate latency and throughput of interconnection architecture in addition to the communication functions we were able to compare the performance characteristics of our hybrid interconnect where a large mesh is broken into smaller meshes, globally connected by a STAR-RING hybrid topology for routing global traffic.

## 2. Related works

In order to find a tradeoff between the resource requirements and system performance in term of surface, reduced hop counts and throughput, a new Network on Chip topologies has been proposed such as hierarchic and hybrid topologies. These networks has been proposed and compared in terms of latency, throughput, and energy dissipation [13], [14].

In [15], an optimal Network on Chip topology which uses the star graphs has been proposed as building blocks. It uses a hierarchical star topology based on star graph. Compared to many topologies in the same category in terms of various performance metrics (diameter, cost, fault tolerance, fault diameter), the hierarchical star topology showed the most energy-efficient and cost-effective topology.

To reduce the latency of long distance traffic in normal mesh 2D, a STAR-TYPE architecture [16] topology has been proposed. It consist to divide an original mesh to 3x3 sub mesh connected together at the central node forming the star topology to form the second-level mesh and using a simple routing algorithm with deadlock-free routing. Compared to normal mesh 2D, the proposed topology presents a good improvement in terms of hop-count reduction which can reach 60, 87% but the drawback of star type architecture is that it consumes more power and area of 34.27% and 57.54% respectively.

A Generic and Extensible SPIDERGON NoC has been proposed in [17]. It is based on elementary asynchronous SPIDERGON network which is a combination of the star

and the ring architectures. The set of elementary Spidergon networks are organized as a two order matrixes. The proposed architecture is characterized by the lower latency and the later saturation, but it suffers from it's over costs in terms of silicon area.

The Proteo [18] Network on Chip is divided into clusters, using a hierarchical network. It comprises multiple subnets with different performance, topologies and packet formats. The hierarchical network built from a system-wide bidirectional ring and several subnets with star (or bus) topology.

In order to smooth and evenly distribute the flow of communication traffic, Ring Road [19] topology has been proposed to avoid congestion in the center by forcing some traffic to take a detour around the center, using ring switching elements to provide more bisectonal bandwidth.

To reduce energy consumption, authors in [20], benefited from the scalability, modularity, and energy efficiency of hierarchical ring. Two-level hierarchical ring interconnect was modeled and evaluated for SoC multiprocessor systems. This topology was inspired by a NUMachine multiprocessor described in [21]. The proposed multi processors NUMachine uses a hierarchical ring based interconnect. This architecture is composed by local and central rings that are joined by inter-ring interface allowing the construction of a modular system with parallel computing capability and cost efficient feature. In [22] through the proposed hybrid Mesh based Star topology an improvement of throughput and low hop count latency was shown compared to SD2D [23], L2STAR [24] and original mesh.

To benefit it from the advantage of mesh topology for short distance traffic, and the advantage of star topology for long distance traffic, author in [25] has proposed a 2D Hybrid Mesh based on Star topology to connect locally mesh and globally star. The proposed architecture improves system performance in term of maximum latency of 62% and increase of 48% in throughput compared to simple 2D mesh under static routing.

In [26] a scalable and heterogeneous NoC with Star-Wheels topology has been proposed which combine the star topology with the Wheel topology (star and the Spidergon topology) utilizing packet switching for controlling data and circuit-switching for an image processing application.

To overcome the problem of Mesh topology, a large communication radius and hot spots have been developed in the center of the Mesh. Authors in [27] have proposed a hybrid ring/mesh architecture, which use a large mesh topology partitioned into smaller sub-meshes for local routing and a hierarchical ring interconnect for global routing of smaller sub-meshes.

For high performance network-on chip, A Scalable hierarchical architecture based Code-Division Multiple

Access (CDMA) has been proposed in [28]. A large network can be obtained, by scaling the local switch architecture. This work is based on CDMA switch in the center for the unicast and multicast data between the IPs blocks. This architecture has presented an average improvement of 24.2% in area cost with a reduction of 25% in the power consumption compared to the conventional design.

In [29], a multicast network-on-chip has been proposed using a combination of hierarchical star and ring topology to support a real-time object recognition processor that supports less than 3 switches hop latency. The proposed architecture has shown an improvement in term of data transaction time and energy consumption by 20% and 23% respectively.

In [30], a hybrid mesh-ring topology has been proposed. It consists of some local mesh networks connected together through a global ring network. Each type of network includes a monitoring system to balance the network load over the communication resources by observing traffic in the network and delivering traffic information to the routers.

To provide the communication of multiple processor elements with high computing performance, a novel hybrid topology STAR- Wheel was proposed in [26]. Both packet switching and circuit-switching were used as communication protocol for data control and data application respectively.

A new NoC with hybrid topology has been proposed in [32]. It is a hybrid of mesh, torus and folded torus. The proposed topology consists of three kinds of links, torus links, folded torus links, and mesh links with a uniform router. However, a significant reduction of the number of average hops-count and an increase of throughput compared to mesh, torus and folded torus topologies was presented.

To provide low latency, higher throughput, and good balancing load network, a 2D hybrid mesh based star topology has been proposed in [25]. by using two different types of connections at different levels, the proposed topology facilitates both long distance traffic and short distance traffic and has presented an improvement of low latency and an increasing throughput by 62% and 48% respectively compared to simple mesh2D.

To reduce the communication overhead for performance, we propose an approach to restrict the communication to a small set of nodes. To enhance the throughput using dedicated local connections, we suggest in this work a new hybrid topology that integrates the 2D-Mesh, STAR and RING architectures benefiting from the advantage of such communication locality. We identify a hybrid locally mesh globally Star-Ring HLMGSR topology and we evaluate it in terms of throughput, latency and area, at the transactional level with SystemC TLM2.0. The hybrid

topology HLMGSR uses the Star-Ring and mesh graphs as the basic building blocks, and inquires about the topological characteristics of the resulting family of networks.

### 3. Topology Exploration

The topology selection in the design of NoC presents a major preoccupation for its importance in the determination of the structural organization of the network routers and subsequently the evaluation of performance in terms of average latency, the total bandwidth and the implementation roughly cost.

The popular 2D-mesh topology has strength in regularity, scalability and fault tolerance due to link failure. However, it suffers from high transmission latency when the network size increases. On the other hand, the star topology performs well for smaller diameter networks. It can also lead to short average hop distance. In opposition, it represents a bottleneck communication in the center node due to congestion [16].

The ring topology that is characterized by its small degree, show that every node has two neighbors however, the since increasing linearly of its diameter lead to long hope latency. In this work, we try to combine these topologies together in order to benefit from advantages of each topology.

We present a new hybrid Mesh Star-Ring combined topology architectures called HMSR (Hybrid Mesh Star-Ring). HMSR is a hybrid interconnected topology which connects localized subnets with each other via global routers. HMSR use multiples mesh as local networks and use one star-ring topology as global network (LMGSR).

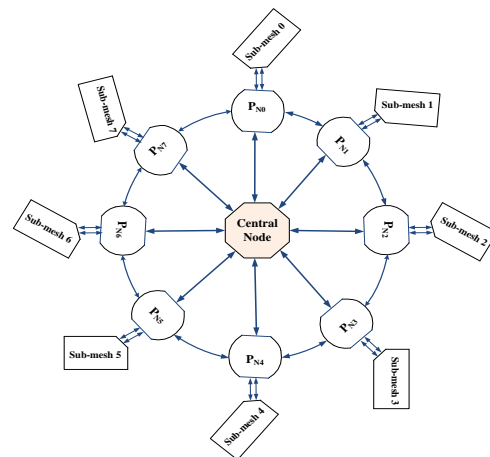


Fig. 1. Hybrid Local Mesh Global Star-Ring topology

### 3.1 HLMGS: Hybrid Locally Mesh Globally Star-Ring topology

The hybrid LMGSR NoC is a communication structure for integrating a very high number of multiple cores and providing highly flexible connectivity at the necessary time. It consists of a local mesh as a subnet and a global Star-Ring network which connects the local sub-meshes as can illustrated in figure 1. Four IPs are attached to four Local Switches (LS) in each subnet and the local switch is connected to one Global Switch (GS).

The router coordinate (0, 0) in the corner of each subnet operates as a router of the mesh to route packets inside the mesh. It also provides the link between these global routers. The corner routers are directly connected to the peripheral Routers of star-ring topology.

The proposed global Star-Ring (SR) topology [11], that is based on star topology adds ring topology for short latency data transmission from the start IP that allow the reduction of the hop count of global long distance traffic.

It's characterized by a diameter of two links regardless of its size. The SR Network is scalable in a way that the number of subnet as well as the number of resources on a subnet can be easily increased. It has three channels so that the packets can be transferred in three directions CW, CCW or CA.

We consider for instance 4x8 mesh topology that supports 32 IP has been divided into eight 2x2 sub-meshes which are globally connected using Star-Ring architecture. Each IP is attached to each local sub-meshes switch (LS). The Local Switch (LS) coordinates (0, 0) in the corners of each sub-meshes is connected to one single global switch (GS) and operates as switches of local sub-meshes network as well as a router to construct a second-level sub-meshes. The structure of the subnet is presented in Figure 2.

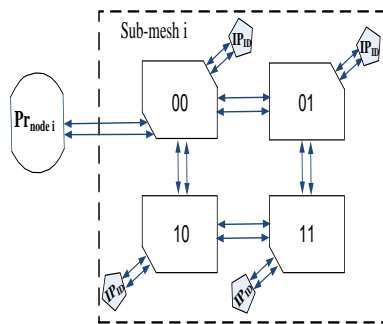


Fig. 2. Local mesh Subnet

Regardless of the type of architecture, Network on chip topologies can be described by a graph  $G(R, C)$ , where  $R$  is the set of routers, and  $C$  is the set of channels between switches [10]. The standard router utilized in the

modulation of different topologies, consists of a routing module, two buffer elements on each channel which receive packets and send them forward as shown in figure3. The routing module is modular in a way that the arbitration method and the routing algorithm can be modified on the function of local subnet size.

In the new HLMGSR topology,  $R$  includes local switches (LS) that provide the intra-subnet switching and global switch (GS) for inter-subnet switching.

The number of core (IPs) can be increased linearly depending on the size of local subnet, where  $M$  and  $N$  represent the width of sub-mesh and  $J$  is the number of global switches on the SR topology.

The number of cores (IP) is calculated by equation (1).

$$Core_{LMGSR} = M \times N \times J \quad (1)$$

The number of routers in Star-ring topology  $V$  (Star-Ring valence) is calculated using equation (2).

$$V = star - ring \ valence + 1 \quad (2)$$

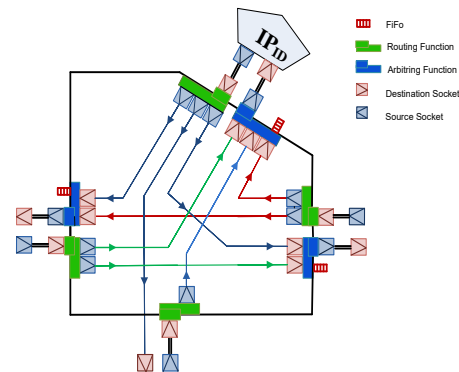


Fig. 3. Internal connectivity of peripheral router

The number of routers (switches)  $K$  in HLMGSR topology is calculated using equation (3)

$$K = [(star - ring \ Valence \times (M \times N) + 1) \quad (3)$$

The Min hop count number in HLMGSR topology is calculated using equation (4).

$$Min - HP = [(M + N) - 2] \quad (4)$$

The max hop count number in HLMGSR is calculated according to equation (5) independently of IP core number

$$Max - HP = [(M + N) - 2] + 2 \quad (5)$$

#### 3.1.1 HLMGSR Addressing

In order to transmit packets of IP cores across the NoC, a unique address must be assigned to each reachable

destination. In both network levels, switches just like IP core have their own unique address as following.

- Source mesh node Address SmNA= (Xs, Ys)
- Destination mesh node Address DmNA= (Xd, Yd)
- Source Star-Ring node Address SSRA= (Ns)
- Destination Star-Ring node Address DSRA= (Nd)
- Distance in X dimension between current node and Destination node  $\Delta x = Xd - Xs$
- Distance in Y dimension between current node and Destination node  $\Delta y = Yd - Ys$
- Distance in global dimension between current SR node and destination SR node:  $\Delta G = Gd - Gs$
- the identification in the global system : id

$$IP_{id} = (m \times n \times Nod_{Star-Ring}) + (X \times m + Y) \quad (6)$$

### 3.1.2 Proposed HLMGSR routing algorithm

In the proposed routing algorithm, each router node position in HLMGSR topology is represented by (X, Y, Gx), where X and Y represent the row and column number of specific local node and Gx represents the source or destination global address of a particular node in a global system.

$\Delta G$ ,  $\Delta x$  and  $\Delta y$  have been used to measure the difference between the source and destination node. When  $|\Delta G|$  are equal to zero, the packet follow local routing, else it follows global routing.

To travel locally, the HLMGSR NoC uses a deterministic X-Y routing on the local sub-meshes networks. Each router on sub-meshes can be identified by its coordinate (x,y). The X-Y algorithm compares the source router address to the destination router address of the packets presented by  $\Delta x$  and  $\Delta y$ .

If  $\Delta x$  and  $\Delta y$  are equal to zero, the packet must be routed to the local port. If this is not the case, the Xd address is firstly compared to Xs address then the packet will be routed to east or west port when  $Xs < Xd$  or  $Xs > Xd$  respectively and if  $Xs = Xd$ .

In the second level, Yd Address is compared to Ys address. The packet will be routed to south when  $Ys < Yd$ , to north when  $Ys > Yd$ .

To send a packet from an initiator to a target connected to remote sub-meshes, the X-Y routing algorithm tends to route global traffic away from the IP sender to the corner router (0, 0) which represents a bridge between the local and global traffic.

When the difference between the source and destination node at global network are not equal to zero  $|\Delta G| \neq 0$ , the packet must follow the global routing. In the global network level, a determinist routing algorithm is adopted while ensuring a communication cost less than or equal to 2 hops regardless of the network size and the STAR

valence. The communication cost is given by the following expression:

$\min [f(\text{way1}), f(\text{way2})] \leq 2$ , where **f** is the cost function in number of links.

The pseudo code of the proposed routing algorithm is as follows:

```

If ( $|\Delta G| = 0$ )
  { //packets travelling on local sub-mesh with XY algorithm
  If ( $\Delta x > 0$  and  $\Delta y > 0$ ) then go to ES;
  Else if ( $\Delta x > 0$  and  $\Delta y = 0$ ) then go to S;
  Else if ( $\Delta x > 0$  and  $\Delta y < 0$ ) then go to WS;
  Else if ( $\Delta x = 0$  and  $\Delta y > 0$ ) then go to E;
  Else if ( $\Delta x = 0$  and  $\Delta y = 0$ ) then go to Local;
  Else if ( $\Delta x = 0$  and  $\Delta y < 0$ ) then go to W;
  Else if ( $\Delta x < 0$  and  $\Delta y > 0$ ) then go to EN;
  Else if ( $\Delta x < 0$  and  $\Delta y = 0$ ) then go to N;
  Else if ( $\Delta x < 0$  and  $\Delta y < 0$ ) then go to WN;
  End if;
  }
Else packets travelling on global Star-Ring algorithm;
End if;
If ( $|\Delta G| \leq 2$ )
  { //-- the global routing algorithm
  If  $|\Delta G| < 0$  then go to clockwise direction;
  Else if  $|\Delta G| > 0$  then go to counter clockwise direction;
  Else if ( $|\Delta G| = 0$  and  $\Delta x = 0$  and  $\Delta y = 0$ ) then go to local of destination sub-meshes corner routers;
  End if;
  }
Else go to the central router in the across direction to reach the destination star-ring routers;
End if;
    
```

### Pseudo-code of the Proposed Algorithm

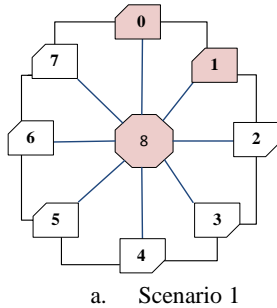
#### 3.1.3 Deadlock avoidance

A deadlock can occur in NoC when different packets will wait for each other for undefined time in a cyclic way [32]. In this study we use deterministic XY routing for local routing, which is a deadlock-free routing algorithm.

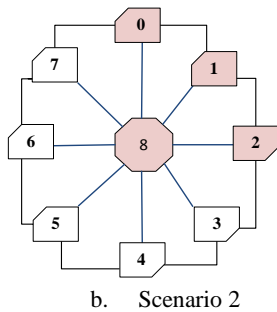
For global routing, the problem of infinite waiting path for wormhole routing can occur during the even cycle such as the example of routers 0, 1, and 8 which can communicate together. Prohibiting certain turns in global network, we can avoid this kind of deadlock.

The routing algorithm would be to prohibit at least one turn in each of some possible cycles in the network. Thus, it can avoid a path between each pair of nodes as illustrated in figure 5, but it should not prohibit more laps than necessary. Interruption of communications, manifested by prohibiting turns CW-AC and CCW-AC.

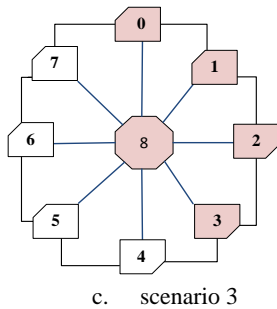
As shown in Figure 4 for the steps of value 1 or 2, the decision function returns a value less than or equal to 2 for calculating the cost of communication intra-ring and inter-Ring. On the other hand, with steps values greater than two, the routing is done through the central node



S0 → D1. First way (0, 8, 1),  $f(\text{way1}) = 2$ .  
 Second way (0, 1),  $f(\text{way 2}) = 1$ .  
 Min [ $f(\text{way 1}), f(\text{way 2})$ ] = 1.



S0 → D2, First way (0, 8, 2),  $f(\text{way1}) = 2$ .  
 Second way (0, 1, 2),  $f(\text{way 2}) = 2$ .  
 Min [ $f(\text{way 1}), f(\text{way 2})$ ] = 2.



S0 → D3, First way (0, 8, 3),  $f(\text{way1}) = 2$ .  
 Second way (0, 1, 2, 3),  $f(\text{way 2}) = 3$ .  
 Min [ $f(\text{way 1}), f(\text{way 2})$ ] = 2.

Fig. 4. Some scenarios for finding shortest path length with maximal diameter 2

The separation of the communication inter-ring and intra-ring does not allow recovery the deadlock and live-lock problems. Each packet from an input port device in the

central node will be able to be routed throughput ports where it represents the valence of the network.

## 4. Experimental results and discussion

Using N routers scales for classical mesh and proposed hybrids topologies as shown in figure 1 some structural characteristics are analyzed. They comprise degree, diameter, hop count, average minimum hop count, average latency and ideal throughput, and further performance evaluation using TLM2.0.

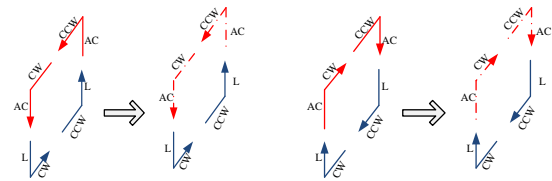


Fig. 5. Showing deadlock avoidance scheme model

### 4.1 Structural proprieties

#### 4.1.1 The degree of the topology

The degree of the topology is the maximum number I/O links associated with the network nodes reflecting the complexity of the topology [15]. The degree of the proposed hybrid topology has uniform degree of all switches except the central node of starring topology which may vary depending on the network size. The maximum degree of the hybrids topologies is limited to 5.

#### 4.1.2 Network diameter

The reduction of network diameter allows the decrease of communication overhead. The network diameter is defined by the largest minimal hop count over all node pairs communicating in the NoC Topology with N node.

$$H_{\max} = \max H(s,d) \quad (13)$$

The diameter of MxN mesh network is (M+N)-2; for the proposed hybrid topology HLMGSR is 4+2 [(M+N)-2] Minimizing the diameter of the network topology in our hybrid network essentially depends on the choice of the locally Mesh network.

The diameter of hybrid topology HLMGSR can decrease by 25% and compared to mesh topology.

### 4.1.3 Ideal average latency

The time required for a packet to traverse the network from source to destination without any congestion in routing is called ideal average latency. This latter can be estimated in formula (14) [33].

$$A_v \text{ latency} = A_{rd} + \frac{D}{v} + \frac{L}{b} \quad (14)$$

$A_{rd}$  is the average router Delay which depends on the average minimal hop count  $H_{min}$  and the delay of single router  $Tr$ , (cycle/hop), knowing that  $Tr$  essentially depend on the physical implementation of the router and the routing algorithm.

$$A_{rd} = H_{min} \times Tr \quad (15)$$

The ratio between the average distance  $D$  from source to destination (hop) that is usually equal to  $H_{min}$ , and wire transmitted speed  $v$  (hop/cycle) represent the transmission time for a network.

The required time to cross a packet of length  $L$  (flit/cycle) via a channel with bandwidth  $b$  is a ration  $L/b$ .

The average minimum hop count of a network represents the average of all possible paths between two node source and destination sources.

$$H_{min} = \frac{1}{N^2} \sum H(s, d) \quad (16)$$

Tableau 1 : calculation of the minimum hop count

Topology	32	64	72	128
Mesh	3,87	5,25	5,58	7,93
HLMGSR	5,12	6,96	6,97	8,81

The average minimum hop count of  $N$  node network varies depending on the larger networks and calculating similarly for the compared topology knowing that each node is considered as source and destination.

The decrease of  $H_{min}$  becomes interesting from network size of 70 nodes. The  $H_{min}$  of HLMGSR is 39% less compared to Mesh at 128 node larger network. While the HLMGSR brought no improvement in term of average minimum hop count.

Assuming a typical 5-stage pipeline router used with the interval time between adjacent pipeline stage is 1 cycle,  $tr = 4$  cycle/ hops,  $V = 1$ flits/cycles,  $L = 2$  flits and  $b = 1$ flits/ cyle. Therefore, the ideal average latencies of Meshes and the proposed hybrid topology are shown in table 2

Tableau 2 : calculation of the ideal average latency

Topology	32	64	72	128
Mesh	21,35	28,25	29,57	41,65
HLMGSR	27,6	36,8	36,85	46

We Remarque that the ideal average latency of hybrid Mesh is less than the HLMGSR topology by average of

28%, but at 128-node scale, the difference of average latency between Mesh and proposed HLMGSR topology decreased at 10%.

### 4.1.4 Ideal Throughput

Adopting the bisection parameter of network (eq. 17) we can estimate the ideal throughput of a topology, determining the maximum throughput in a perfect flow control and routing mechanism [32].

$$T_h \leq \frac{2 \times b \times B_c}{Nodes\ numbers} \quad (17)$$

$B_c$  is the channel count required to portioning the network nearly in half  $b$  is the width of a network.

Tableau 3 : calculation of the ideal throuput

Topology	32	64	72	128
Mesh	0,5b	0,5b	0,4b	0,25b
HLMGSR	0,75b	0,375b	0,3b	0,187b

The ideal throughput of hybrid topology HLMGSR is characterized by a slightly throughput stability compared to the mesh, when increasing the network scales.

Tableau 4 : performance comparison against Mesh topology (128 nodes)

Topology	Average Minimum Hop Count	Average Latency	Idial Throughput
HLMGSR	+11%	+10,4%	+33%

The performance comparison of proposed hybrid topology at 128 nodes is illustrated in Table 4. The Average minimum hop count is risen by 11% for the HLMGSR topology when compared to Mesh. The average latency is increase by 10,4% for the HLMGSR when compared to Mesh topology. The best throughput of hybrid topology HLMGSR increases by 33% when compared to mesh architecture.

### 4.2 Cost and Performance evaluation

In this section the synthesis results will be presented, and a cost analysis of area will be made based on the synthesis results. The proposed hybrid topology performance will be evaluated in terms of latency, and throughput.

The first implementation of NoC uses a HLMGSR topology. The second uses the Mesh topology. It use a network interfaces with 32 bit AHB data fields and 32 bit network ports.

The proposed topology has been modeled with VHDL language at RTL level in order to estimate the cost in term of area. It was simulated and synthesized respectively by using the ModelSim tool and Synopsys Design Vision tool.

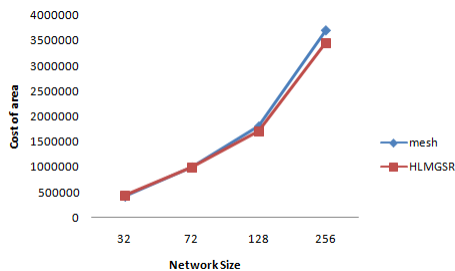


Fig. 6. Comparison area cost of NoCs Architectures

We synthesized the proposed hybrid networks topology using cell based design with ST 0.13nm CMOS technology using the High Speed (HS) library. Furthermore, due to the high pin count, the experimental results are based on the circuit simulation of the design instead of the manufactured chip. The synthesis result of these networks was done with the utilized FIFO have a depth of 4 words of 32 bits. Each FIFO has an adjustable depth and width. Figure 7 shows the area of the three implementations with different network sizes (number of IP cores).

For a network size greater than 72, the area occupied by the HLMGSR network is the most reduced compared to mesh topology. The area increase is about 7% between HLMGSR and Mesh topology.

To complete the performance evaluation, a baseline routers of the Mesh, HLMGSR has been modeled with systemC TLM (transaction level modeling) [20], using an object-oriented style. The library used has been described as a network switch, communication socket, and network wrapper to evaluate the topology in terms of latency, throughput, and area. Plugging building components together provides a way for automatic generating of standard or new hybrid topology with different sizes.

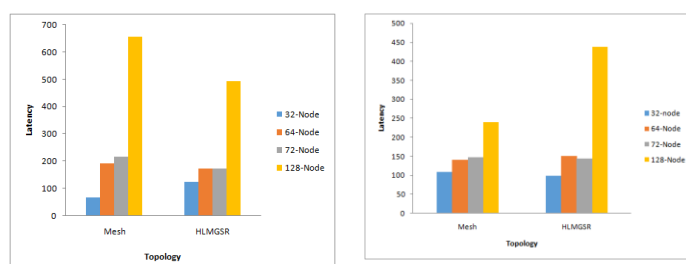
The aim is to evaluate whether the average latency and the throughput for our presented hybrid topology are significantly reduced and increased respectively compared with that of Mesh. We show also that the hybrid topology is able to adapt to a variety of pattern traffic and support different number of IP cores.

We compared the proposed hybrid topology with standard Mesh in terms of latency and throughput with different injection rate, different network sizes and different traffic patterns. The number of IP core used determines the size of network that can be used for mapping the application target to NoC. We proposed to evaluate the presented topologies for different network sizes (32, 64, 72, and 128). The sub network SR is fixed with valence equal to 8. For HLMGSR topology, we used 8 mesh sub network for local communication with different sizes 2x2, 4x2, 3x3, 4x4 to construct respectively 32, 64, 72, and 128 sizes. For Mesh topology, we use 4x8, 8x8, 8x9, and 16x8 to construct respectively 32, 64, 72, and 128 sizes. For performance evaluation, we used the two most traffic patterns used in

the literature such as uniform traffic (UT) and transpose traffic (TT) for different injection rates (0,1; 0,7; 1) and we expect applications to lie in between these two traffic patterns. Figure 7 (a-f) shows the histogram of the average latency of the two topologies for various network sizes. We tried out three injection rates 0,1; 0,7 ;1 (packet/node/cycle) respectively correspond to the sub-graph (a), (b) and (c) for the transpose traffic patterns and (d), (e) and (f) for the uniform traffic patterns.

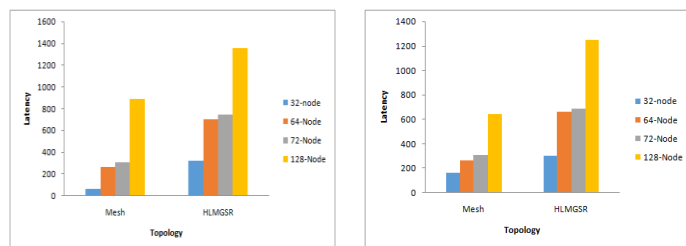
From the histogram, it is clear that for the transpose traffic and for a network size lower than 64 nodes, the Mesh topology provides the lower average latency for the different injection rates.

Average Latency under transpose traffic      Average Latency under Uniform traffic



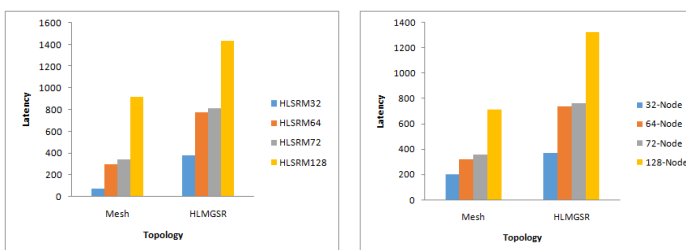
a. Injection rate= 0.1(packet/node/cycle)

d. Injection rate= 0.1(packet/node/cycle)



b. Injection rate= 0.7(packet/node/cycle)

e. Injection rate= 0.7(packet/node/cycle)



c. Injection rate= 1(packet/node/cycle)

f. Injection rate= 1(packet/node/cycle)

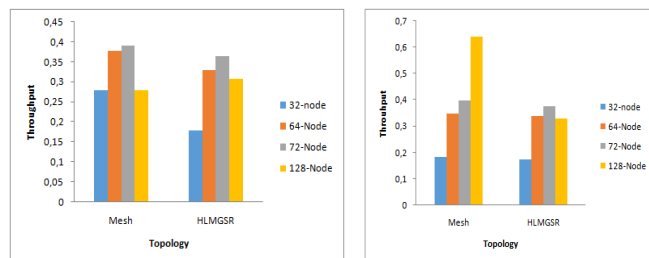
Fig. 7. Latency versus injection rate obtained by uniforme and transpose traffic



It is also clear that for uniform traffic and for a high injection rate, the Mesh topology provides the lowest average latency. For lower injection rate, and for a network size lower than 64 nodes, the HLMGSR topology provides the lowest average latency.

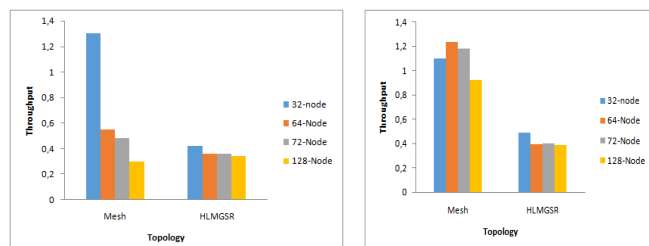
Figure 8 shows the histogram of the throughput of the two topologies and various network sizes. We experimented with three injection rates for the two traffic patterns.

Throughput under transpose traffic      Throughput under Uniform traffic



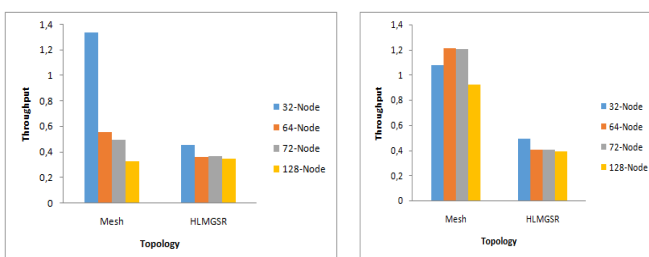
a. Injection rate= 0.1(packets/node/cycle)

d. Injection rate= 0.1(packets/node/cycle)



b. Injection rate= 0.7(packets/node/cycle)

e. Injection rate= 0.7(packets/node/cycle)



c. Injection rate= 1/packets/node/cycle

f. Injection rate= 1/packets/node/cycle

Fig. 8. Throughput versus injection rate obtained by uniforme and transpose traffic

It is clear from the histogram, that for a network size greater or equal to 64 nodes with the transpose traffic pattern, the best throughput is provided by the HLMGSR for different injection rates.

For higher injection rate the HLMGSR provides the highest throughput.

## 5. Conclusion

In this work, we investigate communication locality between MSR and 2D mesh. we have presented a new hybrid topology Hybrid local mesh global star-ring (HLMGSR) with the shortest path routing algorithm.

We evaluated and compared the hybrid topology against mesh NoC topology for various network sizes and workloads. The experimental result show that for a network size equal to 128, the proposed hierarchical topology HLMGSR provides an area 7% over the mesh. For a network size greater or equal to 64 nodes, the lowest average latency is provided by the proposed hybrid topology for different injection rates. The results show that for a network size greater or equal to 64 nodes with the uniform traffic pattern with a lower injection rate, the best throughput is provided by the HLSRGM, but for higher injection rate the HLMGSR provides the highest throughput.

To conclude, this paper aims at designing communication locality aware hybrid networks that the performance of a hybrid topology can be improved further by making use of more intelligent schemes for preserving locality in large SoC systems.

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