Optimization of Power Consumption in VLSI Circuit

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Abstract

Space, power consumption and speed are major design issues in VLSI circuit. The design component has conflicting affect on overall performance of circuits. An optimization of power dissipation can be achieved by compromising various components. Power consumption in VLSI circuit (like in multipliers) is also data dependent. In this paper attempt has been made to test different design methods and propose a modular approach for optimizing power consumption. It is found that algorithm based design reduce gate switching activity considerably and as result power consumption in multiplier is reduced.

Keywords: *Genetic Algorithm, Booth Multiplication, Power Optimization.*

Introduction

Reduction in Power dissipation is an essential design issue in VLSI circuit. The design parameters have conflicting affect on overall performance of the system. Depending upon the component and function, different optimization approaches can be adopted. For instance power consumption in multiplier is data dependent as gate switching activity contribute to more power consumption. The gate switching activity can be optimized by considering different gate combinations. Gate switching activity can be reduced by employing various algorithms. For instance, in multiplier, design method used for multiplication have affect on power consumption. In multiplier, besides primary school method of bit multiplication, Booth algorithm & Modified Booth algorithm can be used for efficient multiplication.

Gate level design of circuit may be used to opt various combinations of circuit and associated power consumption. Genetic Algorithm can be effectively used to explore different combinational circuits. In this paper various approaches are surveyed for power consumption in VLSI circuits. As a test case multiplier circuit is used to study various approaches

Dynamics of Power Consumption

Power dissipation in VLSI circuits is due to three major sources i.e., power required to charge or discharge a node, power dissipation due to output transition and power dissipation due to leakage current. So optimizations can be achieved by concentrating any one or combination of above design issues. The power consumption can be given by following equation:

$$P_g = f^g C_{sc} V_{dd}^2 \quad \text{----------(Eq. } a\text{) [11]}$$

Where,

P_g = Power consumed by a single gate
f^g = Average operating frequency of the gate
C_{sc} = Switching capacitance of the gate
V_{dd}^2 = Power supply voltage

Using (Eq. *b*) is obtained from (Eq. *a);* for any number of gates in the chip.

$$P_g = N f^g C_{sc} V_{dd}^2 \quad \text{---------(Eq. } b\text{) [11]}$$

Where,

$N f^g$, represent the total number of bit-operations per second.

Power dissipation estimation

In all logic circuits, power consumption is related to information transfer and each circuit have inherent requirement of information transfer. Let ***R*** is the transfer rate requirement for a given architecture; the lower bound of this rate may be determined which consequently can be used for power dissipation estimation. The different digital architecture can perform same function but may have different information transfer rate and different channel capacity. Channel capacity can be given as:

$$C = \int_0^W log_2[1 + SNR(f)]df$$

---------**(Eq. *c*) [12]**

Where, SNR gives signal to noise ratio. For any meaningful transfer capacity should be greater or equal to R. The overall noise power in digital circuit is a function of signal power, temperature, semi conductor property etc. However, power dissipation is mainly due to ground bounce. The lower bound of the power dissipation can be calculated using information transfer capacity of channel. Let *R* is required information transfer, *W* is the channel bandwidth, sigma be noise power and *C* is channel capacity. Using (Eq. *c*) and (Eq. *d*)**,** lower bound of power dissipation can be given as:

$$P_{D1,min,ser} = C_L \left(2^{\frac{R}{W}} - 1\right) 8 \sigma_N^2 W$$

---------**(Eq. *d*) [12]**

Data Dependent Power Optimization

Complexity of data contributes to gate switching activity in the circuit. By adopting efficient computation algorithm design components of the circuit at gate level can be reduced. Investigating different designs & arithmetic representations might reduce power variations. Model can be built to simulate power consumption.

By applying simulation to standard designs and comparing with optimum, better design component can be found. Gate switching for all initial states and all inputs can be simulated to analyze power consumption in each option. Data dependence consideration is helpful in gate design complexity. Ordering of gate inputs affect both power and delay. Parsed [1] has described methods to optimize the power and/or delay of logic-gates based on transistor reordering. Therefore, considerable improvements in power and delay can be obtained by proper ordering of transistors. For instance, late arriving signals can be placed closer to the output to minimize gate propagation delay.

Another approach to reduce power is to consider the size of gate, which has significant impact on circuit delay and power dissipation. By increasing the size of transistors in a given gate, delay of the gate can be decreased but in contrast, power dissipated in the gate and fabrication space increases. Therefore, an optimum balance can be achieved by sizing of transistors appropriately. A method is to compute the slack at each gate in the circuit, where the slack of a gate corresponds to how much the gate can be slowed down without affecting the critical delay of the circuit. Alternatively, in different sub – circuits, where slack is greater than zero are utilized and the size of the transistors is reduced until the slack becomes zero, or the transistors attain a minimum size.

Combinational Gate Level Design

In gate level design of circuit, different combination of logical gates may produce same circuit output but different value of power consumption. Path balancing, factorization and don't care optimization may be utilized to optimize power consumption. Path balancing can be achieved by avoiding delay at each input gate.

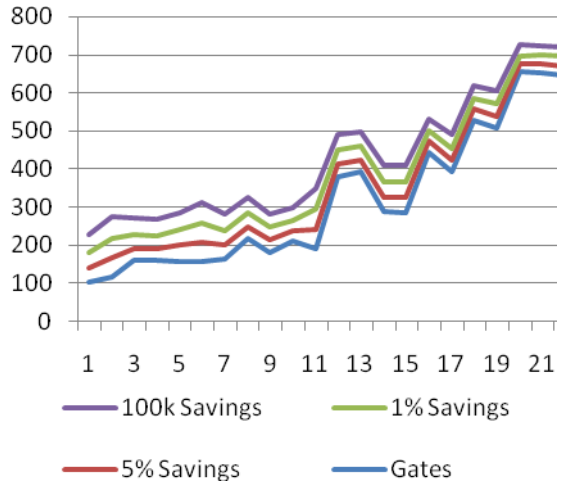
Genetic Algorithm can be used to determine different combination of gates and power consumption can be formulated by devising *Fitness Function.* Coello et. al. [3] has proposed design of combinational logic circuit based on Genetic Algorithm. By defining chromosome development

scheme of various combinations of logic circuits can be evolved using *cross over* and *mutation*. This approach is more efficient (in some particular scenarios & constraints) than human designer as various constraints of design circuit can be devised subject to fitness function.

Genetic Algorithm can reduce number of gates, which consequently reduce power consumption; as the work of Coello et. al. [2], shows on 2-bit adder and 2-bit multiplier with a particular 'cardinality' [2]; about 56% reduction in number of gates for the circuit can be achieved.

NUMBER OF GATES VERSUS POWER SAVING IN CMOS – BASED ON ISCAS-89 BENCHMARK CIRCUITS [8]

It is very obvious that number of gates is directly proportional to the power consumed; as shown in the (***Graph-1)***. So, if we minimize the number of gates in the design we can achieve low power consumption as well; as Coello et. al. [2] proposed.



(*Graph-1) Gate Vs Power based on the work of Jonathan P. Halter and Farid N. Najm* [8]

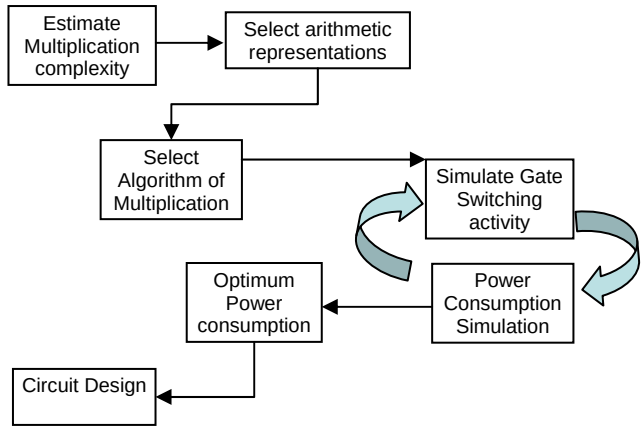
On the other hand power reduction is sometimes a ***"Give n Take"*** scenario; if we achieve reduction in power supplied there may be some loss in speed, efficiency etc., and so, minimizing power without losing other recourse parameters is the need of time.

(Table-1) Power reduction versus Speed loss

Power Reduction in supply voltage	Speed Loss	Constraints/ Specifications
leakage power reductions up to 54%	Not reported	"Logic design to reduce the leakage power of CMOS circuits that use clock gating to reduce the dynamic power dissipation tested on ISCAS-89 benchmark circuits" **[8]**
0.13 V or 800 times	19 times	"0.5-fim gate length and static logic" **[9]**
"1.1 V supply and consumes less than 5 mW-which is more than three orders of magnitude lower power compared to equivalent commercial solutions." **[10]**	Not reported	---

Discussion

For instance, a modular approach as shown in (***Fig. 1)*** is proposed to adopt appropriate optimization technique considering different possibilities in multiplier design.



(*Fig. 1)* Modular approach of Multiplier Design

It is found that data complexity and various combination of gate level digital circuit has considerable impact in power dissipation. Beside this physical design of the chip can be optimized by using Genetic Algorithm by analyzing placement option; subject to optimum space allocation. Similarly selection of Booth Algorithm and Modified Booth Algorithm may reduce power consumption as consequence of data complexity. It is found that in multiplier circuit, Modified Booth Algorithm reduces power consumption as compared to other methods of multiplication.

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