A Technique to Reduce Transition Energy for Data-Bus in DSM Technology

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Abstract

As CMOS VLSI integration continues with shrinking feature size, the energy dissipation on the on-chip data buses and long interconnects becoming a bottle neck for high performance integrated circuits. This energy dissipation is due to increase in inter-wire capacitance. This capacitance on on-chip data buses and long interconnects plays an important role in the reliability and performance of the system. These on-chip data buses consumes major portion of wiring energy. Hence this energy dissipation can be reduced by encoding the data on the data bus. Hence transition energy reduction data bus encoding scheme is proposed which can reduce the energy dissipation on on-chip data buses. The proposed technique can able to reduce the energy dissipation by 42% to 47% for 8-bit, 16-bit, 32-bit and 64-bit data buses compare with unencoded data and 1% to 26% more compare with other existing techniques.

Keywords: *CMOS, Inter-wire capacitance, VLSI, Feature size, Data bus, interconnects, energy dissipation*

1. Introduction

As CMOS technology progresses into DSM and VDSM, it poses many challenges to design and test engineers. The scaling of VLSI integrated Circuits has increased the sensitivity of CMOS technology to cause large energy dissipation, propagation delays and various noise mechanisms such as power supply noise, crosstalk noise, leakage noise, etc. Most of the energy is being wasted on the data buses and long interconnects as dynamic energy dissipation for charging and discharging of internal node capacitances and inter-wire capacitances.

Unfortunately in nanometer and sub nanometer technologies the inter wire capacitance dominates the substrate capacitance and its magnitude is several times larger than load capacitance. The power consumption of on-chip wiring occupies a significant portion of total chip power consumption. In fact it is about 50% of total chip power consumption [12]. It has been estimated that more than 30% of on-chip wiring power consumption is due to data buses and long interconnects and that fraction is growing with technology scaling. The characteristics of data buses and long interconnects such as wire spacing [9], wire length, wire material, wire width, driver strength, coupling length and signal transition time, etc. influences the coupling effect. This increased inter wire effect on on-chip buses and on long interconnects not only increase the energy dissipation but also deteriorate the signal integrity due to the inter wire capacitance. Reducing the energy consuming transitions can also reduce the crosstalk and delay faults [11], [17]. The coupling capacitance also depends upon the data d ependent transitions and the coupling effect will increase or decrease depending upon the relative switching activity between adjacent bus wires [18]. Hence reducing switching activity eventually reduces the energy dissipation.

Transition activity on the data bus can be reduced by employing bus encoding techniques. Several bus encoding techniques have been proposed to reduce energy consumption during bus transmission in literature. These techniques mainly relay on reducing the data bus activity by decreasing self transitions or transitions due to inter wire capacitance. Reducing power consuming transition by encoding the data on the data buses leads to reducing the bus activity hence overall power is saved.

Over the past few years, a n umber of coding techniques have been proposed for reducing the transitions on a data bus. For data buses, one popular coding scheme is the bus invert coding technique proposed by Stan and Burleson [1]. Other variants of the bus invert coding schemes include a decomposition approach [5] and partial bus coding technique [6]. The energy dissipated due to coupling capacitance is analyzed in [7], [8], [10], [19],[14]. For instruction buses Gray code [2], T0 code [3], the Beach code [4] have been proposed which reduces the transitions there by reducing the power dissipation. In almost all above mentions methods either coupling transitions or self transitions are considered [16]. The proposed method by using Bus regrouping with Hamming distance considers both coupling as well as self transition which results to a more save in energy dissipation.

2. Energy Dissipation of a Data Bus

Data buses and Interconnect design play an important role in modern VLSI systems by providing a communication medium between long distant points having low latency, small energy consumption, reliable and robustness against different noise mechanisms. An important figure of merit for data buses and long interconnects is the energy consumption [13], which is a function of the routing materials, the bus topology and technology parameters. The approximate energy expression for the self transitions and coupling transitions considering lumped model of the bus is analyzed by Sotiriadis and Chandrakasan [9]. For the 3-bit data bus the same lumped model is considered here. Energy expression for 3-bit data bus can be expressed as

$$E_1 = C_L \cdot \{(1+\lambda)\cdot(V_1^f - V_1^i) - \lambda\cdot(V_2^f - V_2^i)\}\cdot V_1^f \quad (1)$$

$$E_2 = C_L \cdot \{-\lambda\cdot(V_1^f - V_1^i) + (1+2\lambda)\cdot(V_2^f - V_2^i)\} - \lambda\cdot(V_3^f - V_3^i)\cdot V_2^f \quad (2)$$

$$E_3 = C_L \cdot \{-\lambda\cdot(V_2^f - V_2^i)\} + (1+\lambda)\cdot(V_3^f - V_3^i)\cdot V_3^f \quad (3)$$

$$E = E_1 + E_2 + E_3 \quad (4)$$

Where V_1^f, V_2^f and V_3^f are final voltages and V_1^i, V_2^i and V_3^i are the initial voltages of the 3-bit data bus wires respectively. V_1^f, V_2^f, V_3^f, V_1^i, V_2^i and V_3^i can be either V_{dd} or Ground potential. Combining the eq.1, eq.2 and eq.3 the total energy can be calculated as in eq.4..E_1, E_2, and E_3 represent energy for wires 1, 2 and 3, respectively. For a 0.18 nm CMOS technology and minimum distance between wires, the ratio of coupled capacitance (C_I) to substrate capacitance (C_L) is $\lambda = \frac{C_I}{C_L} = 3.2$.[7] The energy saved due to the reduction of transitions is given in [17] as

$$\text{Energy saved} = \left(1 - \frac{E_{UNC}}{E_{COD}}\right) * 100 \quad (5)$$

Where E_{UNC} is the energy dissipated due to unencoded data transitions and E_{COD} is the energy dissipated due to coded data transitions.

3. Energy Efficient Data Bus Encoding Scheme

The proposed energy efficient encoding technique is based on the number of coupling transitions occurring on the data bus when a new data is to be transmitted. In the following analysis assume 8-bit data bus i.e n=8. By using the following algorithm energy due to transitions can be reduced. The proposed algorithm for 8-bit Data bus is given as follows:

Let 8-bit data bus be represented by

$d_0\, d_1\, d_2\, d_3\, d_4\, d_5\, d_6\, d_7$

- Calculate the number of CT (coupling transitions) of the present bus data with the previous bus data.
- Calculate the number of ST (Self transitions) of the present bus data with the previous bus data.
- Calculate the energy dissipation due to self and coupling transitions.
- If CT >= (n/2) then
- Consider the grouping of the present bus data. Now arrange the data on the data bus as

  Odd Group: $d_0d_2d_4d_6$

  Even Group: $d_1d_3d_5d_7$
- The Hamming Distance between odd group of present data and odd group of previous data is calculated. This is represented as OHD = Odd bits Hamming Distance
- The Hamming Distance between even group of present data and even group of previous data is calculated. This is represented as EHD = Even bits Hamming Distance
- Transmit the data by following the below conditions:

  If OHD > EHD, flip the data in odd bit positions and append bit '1' on the left and bit '0' on the right side of the encoded data.

  If EHD > OHD, flip the data in even bit positions and append bit '0' on the left and bit '1' on the right side of the encoded data.

  If OHD = EHD, flip the entire data and append bit '1' on the left and bit '1' on the right side of the encoded data.

- If CT<n/2 is true then transmits the data as it is, append bit '0' on the left and bit '0' on the right side of the encoded data.
- Calculate the coupling and self transitions of transmitted encoded data with present transmitting encoded data.
- Calculate the energy dissipation due to self and coupling transitions of encoded data.

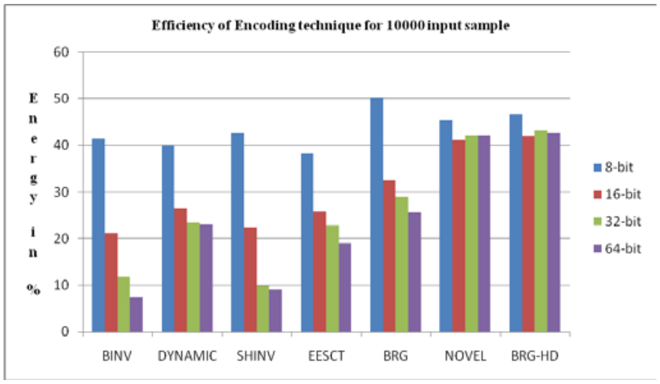

Fig. 1. Comparison of Efficiency of different encoding techniques for 10000 inputs for different bus widths

Table 1: Energy saving (in %)of different encoding techniques

METHOD	8-bit	16-bit	32-bit	64-bit
BINV	41.372	21.233	11.827	7.357
DYNAMIC	39.922	26.524	23.426	22.986
SHINV	42.732	22.430	9.7903	9.127
EESCT	38.399	25.725	22.876	19.021
BRG	50.183	32.472	28.929	25.643
NOVEL	45.347	41.189	42.165	42.150
BRG-HD	46.614	42.086	43.219	42.721

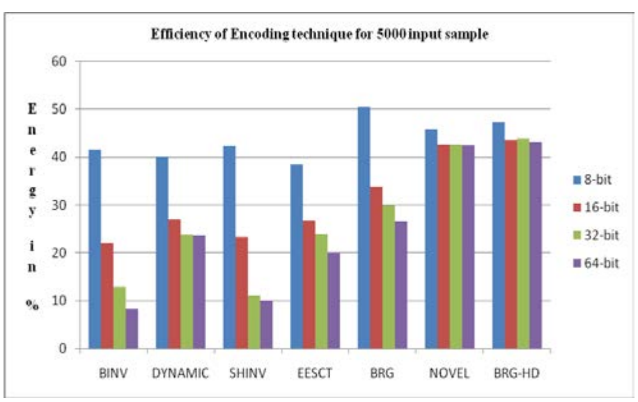

Fig. 2. Comparison of Efficiency of different encoding techniques for 5000 inputs for different bus widths.

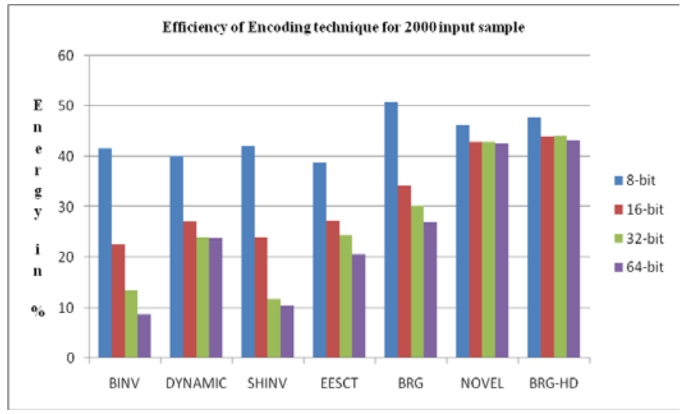

Fig. 3. Comparison of Efficiency of different encoding techniques for 2000 inputs for different bus widths.

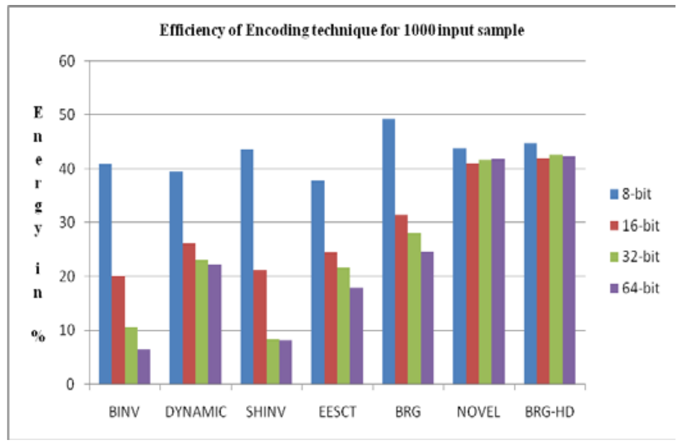

Fig. 4. Comparison of Efficiency of different encoding techniques for 1000 inputs for different bus widths.

4. Performance of the Proposed Technique

The proposed technique performance is compared with other six existed methods. The simulations are performed on 8-bit, 16-bit, 32-bit and 64-bit data buses with three groups of 1000, 2000, 5000 and 10000 data vectors. Self transitions and Coupling transitions are considered as metric parameters. Self and coupling transitions are separately calculated. Energy saved is calculated based on the expression given in [18] and for 180nm CMOS technology, $\lambda = 3.2$ [7]. It shown in Table I that the energy saved using eq.5 on data bus is about 42% to 47% compared to unencoded data transitions. The main advantage of proposed technique is that its efficiency in reduction of energy dissipation is consistence as the bus width varies from 8-bit to 64-bit apart from Novel encoding technique. Other technique's energy efficiency reduces as the bus width increases. This can be seen from Fig-1 to Fig.4. BRG is the best energy efficient technique for 8-bit data bus only. The proposed encoding technique performance is compared with Bus invert(BINV)[1], Dynamic encoding

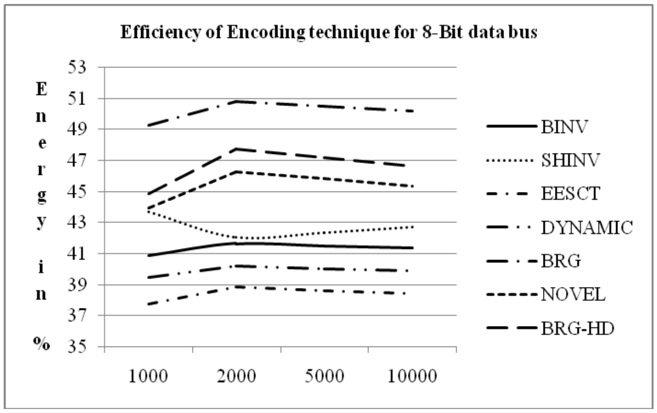

Fig. 5. Comparision of proposed technique with other techniques by varing input sample sizes for 8-bit data bus.

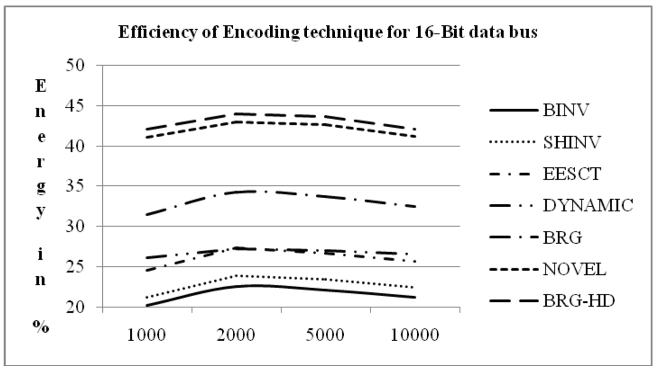

Fig. 6. Comparision of proposed technique with other techniques by varing input sample sizes for 16-bit data bus.

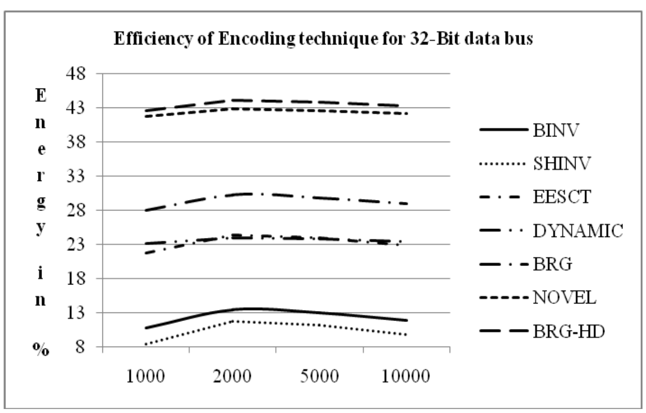

Fig. 7. Comparision of proposed technique with other techniques by varing input sample sizes for 32-bit data bus.

technique (DYNAMIC)[10], Bus regrouping (BRG)[19], Shift invert (SHINV)[15], Energy efficient spatial coding technique (EESC) [16] and A Novel deep submicron bus coding [14]. Its efficiency is compared with other six techniques by varying input sample sizes and its performance is shown in Fig. 5 to Fig.8. It is observed that the proposed techniue can able to save more energy dissipation than others.

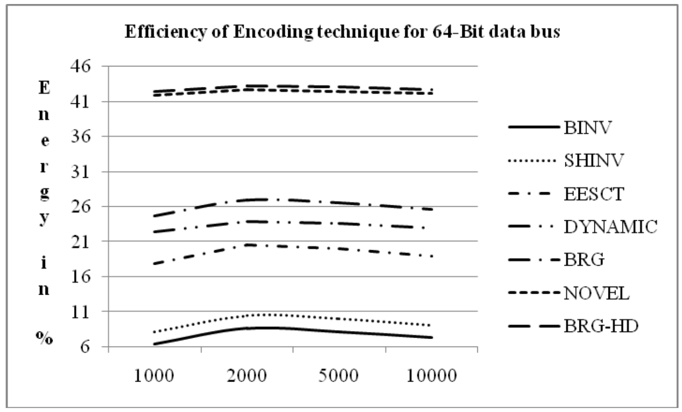

Fig. 8. Comparision of proposed technique with other techniques by varing input sample sizes for 64-bit data bus.

5. Conclusions

The proposed energy saving efficient technique for data bus encoding scheme reduces the power consuming coupling transition as well as the self transitions on data bus transmission in deep sub-micron buses. The main aim of the proposed technique is to save the energy dissipated due to the transitions on data buses. Since coupling transitions are reduced the errors due to crosstalk also reduces. The simulation results show that the proposed technique saves 42% to 47% of energy dissipation for 8-bit, 16-bit, 32-bit and 64-bit data buses compare with un-encoded data and 1% to 26% more compare with other existing techniques. The advantage of the proposed technique is that its energy saving efficiency is consistent with the increase of data bus width.

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