Configuration of FPGA for Computerized Speech/Sound Processing for Bio-Computing Systems

V. Hanuman Kumar and P. Seetha Ramaiah

Department of Computer Science & Systems Engineering,

Andhra University, Visakhapatnam , India, 530003

Abstract

The development of Embedded Computer based bio-computing systems mimicking the natural functionality of human parts, is in continuous research because of advent of technology that used Very Large Scale Integration (VLSI) devices such as Field Programmable Gate Array (FPGA) to meet the challenging requirement of providing 100% functionality of the damaged human parts. The evolution of Field Programmable Gateway Array (FPGA) devices to the current state- of-art System-On-Chip (SOC) devices poses considerable problems in terms of ensuring designer productivity in developing high end Computerized Biomedical Speech Processing applications to these devices. Modern Programmable FPGA structures are equipped with specialized Digital Speech Processing embedded blocks that allow implementing digital speech processing algorithms with use of the methodology known from digital signal processor these programmable FPGA architectures give the designer the possibility to increase efficiency of the designed system. This paper presents the details of design and development of one of the bio-computing systems such as Bionic Ear or Cochlear Implant **(CI)** system with greater emphasis on configuration of FPGA with efficient processing algorithm. Bio-computing system incorporates Xilinx Spartan3 FPGA as the main chip for DSP IP cores, 32k words of memory, a 16-bit Analog to Digital converter fixed gain amplifier and programmable gain amplifier and transmitter which convey control codes to the receiver stimulator of the cochlear implant .The processor is battery powered and has been programmed to emulate the continuous interleaved sampling speech processor of 8 electrode implant. Here the Bio-computing system is a Real-Time Embedded Computing System **(RTECS)** that is required to collect the real-time speech/sound data, process the data by using speech/sound processing algorithm(s) and send the processed speech data to the electrode array inserted in the damaged inner ear (cochlea) for providing the speech recognition to the deafened person via inductive transcutaneous RF link. This process should run continuously without loss of speech/sound information.

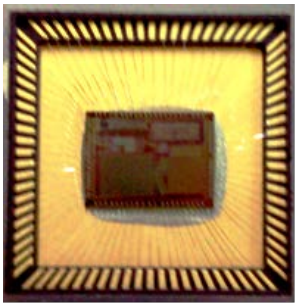
Key words: FPGA, DSP IP, Bio-computing system, Speech Processing algorithm, FPGA VLSI, System-on-chip, RTECS, CI

1. INTRODUCTION

The Bio-computing system comprises of external Body Worn Speech Processor **(BWSP)**, external Impedance Telemetry **(IMT)** and internal Implantable Receiver Stimulator **(IRS)** with an electrode array. BWSP receives an external sound or speech and generates encoded speech data bits for transmission to IRS via radio frequency transcutaneous link for exciting the electrode array by continuously executing speech/sound processing program embedded in BWSP. The IRS receives the ASK modulated encoded speech/sound information, demodulates the ASK signal, decodes the information and stimulates the selected electrode in the electrode array with the appropriate electric stimuli as bi-phasic current pulses by continuously executing decoded speech/sound and electrode stimulation program embedded in IRS to recognize the speech/sound by the deafened person. External IMT is used to measure electrode-tissue impedances of the inserted electrode array inside the damaged cochlea for configuring the number of active electrodes. Commercially available devices are often found to provide little of the flexibility required for use in a research environment, so the need for a fully configurable FPGA based computerized speech/sound processor for use with bio-computing devices is evident. Previously developed portable digital sound processor, referred to as the P-DSP[1], and a modification known as the P-DSP/HA[2], are much larger, heavier and expend more batteries than current commercially available processors. These factors are inconvenient to the hearing-impaired user, and thus may reduce the amount of experience gained by using the processor in everyday conditions away from the laboratory.

(a) BWSP with Headset

(b) Implantable Receiver-Stimulator



(c) Preliminary Version of ASIC Chip for Receiver Stimulator

Figure1: Prototype to Product Development of AU-NSTL Cochlear Implant System

This paper addresses the Design and development of Bio-computing system as a laboratory model based on Xilinx Spartan3 FPGA (1.2V core) as the main chip for DSP IP cores and Micro blaze / Pico blaze microprocessor. The hardware as well as software design and performance issues are also covered in the present paper. The Bio-computing system comprises of the following hardware modules with relevant embedded software control: a) Configurable FPGA for Speech/Sound Processing as BWSP, b) Implantable Receiver-Stimulator and c) Impedance Telemetry.

A configurable FPGA for speech processing consists of a microphone, fixed gain amplifier, programmable Gain amplifier,16-bit ADC, Xilinx Spartan3 FPGA (1.2V core), radio frequency transmitter ,laboratory model of receiver-stimulator and simulated electrode array with a high speed data acquisition system. Figure 1 shows our proposed prototype to product model of Cochlear Implant System designed and developed by AU-NSTL team. The BWSP comprises Ana log Front End (AFE), Digital Speech/Sound Processing system, Speech Data Encoder, and a Radio Frequency Transmitter using Amplitude Shift Keying (ASK) modulation. FPGA can be configured to implement 4-channel to 8-channel **Continuous Interleaved Sampling** (CIS) algorithm based on the patient's active electrodes. This BWSP generates continuous serial TTL data bits based on the voiced or unvoiced signals served as modulating signal to the ASK modulator at 4MHz RF carrier. The ASK signal is applied to the RF transcutaneous link that in turn used to stimulate the Cochlear Implants Implantable Receiver-Stimulator fabricated as laboratory prototype model for testing and validation. The laboratory model of Receiver-Stimulator consists of radio frequency ASK receiver, speech data decoder, stimulus buffer, 8-bit Digital to Ana log Converter(DAC), constant current generator, active electrode selection logic for switch matrix driver, 8-bit Ana log to Digital Converter(ADC), switch matrix based on H-bridge architecture and 12 simulated electrode resistance array. The development of Bio-computing system as per the design has met the requirements of processing real-time speech/sound signals using the principles of embedded computing architecture. The testing and validation of the developed prototype of Bio-computing system is done by start small approach that tests individual functional units followed by an integrated testing. The performance of the developed system is compared with commercially available CI systems and found equivalent performance using relevant test data, simulation tools and emulation tools. The results of experiments with simulated speech/sound test data and real time speech /sound data are enumerated. Finally, the concluding remarks and future directions for an advanced Bio-computing system are addressed.

2. HARDWARE DESIGN

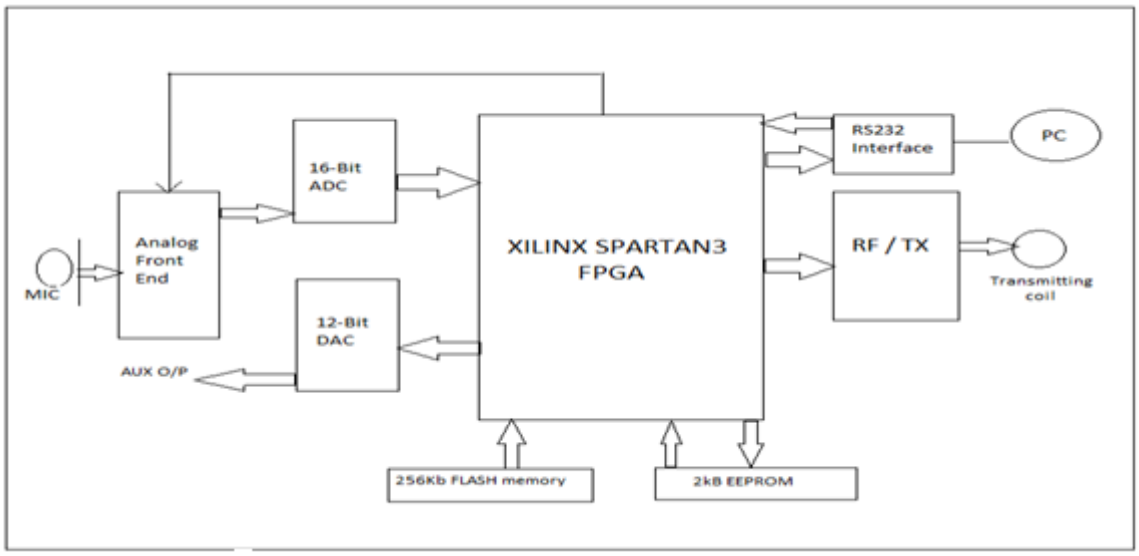


Figure 2: Functional Block Diagram of Configurable FPGA for Bio-computing systems for Speech/sound processing.

The functional components used to configure FPGA for Bio-computing systems can be observed in fig2.Configuration of FPGA for Bio-computing systems to perform speech/sound processing can accept speech or audio signals and transform them into human understandable processed speech or audio to an implantable Bio-computing system's receiver-stimulator of 12 electrodes for making the deaf person to understand the speech or audio tones is designed. The main principle behind the configuration of FPGA involves capturing sound from the environment, processing sound into digital signals and delivering sound to the hearing nerve via electrode array in cochlea. The speech processing system can drive a hearing aid receiver stimulator and excite 8-channel electrode array. In a typical application the system works in the following way.

Sound waves are converted to electrical signals by the microphone and then fed to Ana log Front-end circuit. An electric condenser microphone can be connected to the front panel auxiliary input socket. The sound signals are amplified by fixed gain amplifier with a fixed gain of 30dB and based on volume control of speech processing device, programmable gain amplifier amplifies the output of the fixed gain amplifier and then the signal is attenuated by the sensitivity potentiometer. The signal is filtered to eliminate noise before being converted to a 16-bit digital value by the 16-bit ADC; the 16-bit sample is transmitted to the Xilinx spartan3 FPGA device via a serial interface. The Xilinx spartan3 FPGA typically stores this sample in memory for future processing and may transfer a modified sample back to the SCI to be transmitted to the DAC, where the sample is converted to an Ana log signal to drive a hearing aid receiver. For auditory prostheses use, the Programmable Xilinx spartan3 FPGA based processor periodically construct data frames in the special format required for the cochlear implant receiver

Figure 3: Simplified Block Diagram of the Bio-computing System

stimulator which determines the active electrodes and their current levels and then sends the encoded data frames serially with 171 Kbps rate to the RF transmitter.

The RF transmitter is based on ASK modulation and operates at 4MHz carrier frequency. The RF transmitter modulates the incoming encoded serial data. The encoded data would send to RF transmitting coil. The RF transmitting coil is seventeen turns, 175 strands Litz wire with High Q value. RF transmitter sends the data frames via the transcutaneous inductive coupling to the receiver coil in the laboratory model receiver-stimulator. The receiver stimulator decodes the data and activates the specified electrodes, which stimulate nearby auditory neurons, giving the user the sensation of hearing. A simplified hardware functional block diagram of the Bio-computing system is shown in Figure 3.The Xilinx spartan3 FPGA is used as the central processing system running at a rate of 326 MHz of core clock frequency and Densities as high as 74,880 logic cells. Up to 1872 Kbits of total block RAM ,up to 520Kbits of distributed RAM, Three separate power supplies for the core (1.2V), IOs (1.2V to 3.3V), and Special function(2.5V) eliminating the need for power- consuming external RAM in auditory implant applications. The on-chip peripherals consist of SCI-a Serial Communications Interface, a parallel Host Interface, and a Timer Module and relevant control signals are used to access external memories, as well as the encoder in this application. The required software programs like CIS, ENCODING module stored in an external PROM and these are used by FPGA for speech processing. The mode pin logic levels are automatically altered when the programming cable is connected to the processor. The speech processing Software CIS for DSPMAP is developed in personal computer (PC) using verilog and configured Xilinx spartan3 FPGA using JTAG cable using Xilinx ISE Environment.

3. SOFTWARE DESIGN

There is a huge demand for low cost and high performance of Bio-computing systems in developing countries. Several researchers proposed and attempt to develop a low-cost cochlear implant system but none of these products are available in the market. The development of Bio-computing system involves the strategies of mechanical engineering, physiology, electronics engineering and computer science and engineering. Implementation of embedded speech processing algorithms plays an important role in the development of different techniques for deriving electrical stimuli from the speech signal. Developing speech or sound signal processing algorithms that would help in mimicking the function of a normal cochlea in inner ear is the biggest challenge for the computer engineers. Popular speech processing algorithms such as SMSP, SPEAK, CIS and ACE are used by various vendors are described by the several developers with less technical , design and implementation details due to the limitations of proprietary information or intellectual property rights. The functional block diagram is shown in Figure 4 contains the BWSP, IRS and Electrode array. The Implantable Receiver Stimulator Software decodes the encoded speech signal, generates the required control signals for selection of active electrode for stimulation according to the intensity of the incoming speech/sound signal by means of charge balanced bi-phasic pulses for understanding the speech. The functional block diagram of the Bio-computing system is shown in Figure 5.

Figure 4: Functional Block Diagram of the Cochlear Implant System

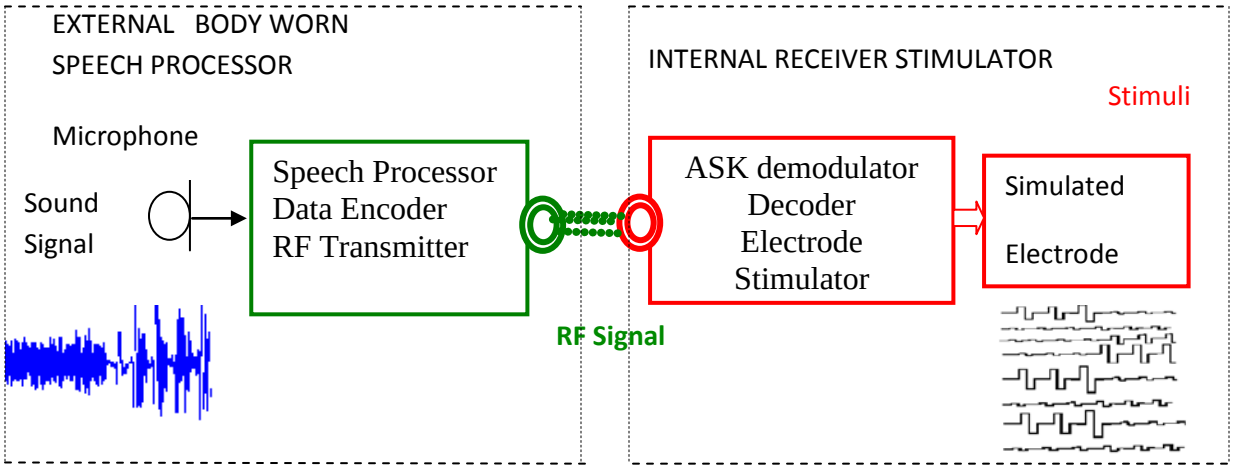


Figure 5: Simplified Functional Block Diagram of Bio-computing

The main functional requirement of the system is to receives the speech/sound signals from the environment and stimulate the electrodes inserted in the cochlea by charge balanced bi-phasic electrical signals. Body Worn Speech Processor receives the electrical signal from the microphone, sampled by CODEC, processed by implementing Continuous interleaved sampling (CIS) speech processing algorithm in FPGA Structures , encoded in using a simple protocol and transmitted serially at 172Kbps rate to the ASK modulated RF transmitter.

Block diagram for 8 –channel CIS implemented in ADSP 2185 is shown in Figure 6. Incoming speech signal is sampled by the ADC is passed to 8 band pass filters. The envelopes of the filtered waveforms are then extracted by full-wave rectification and low-pass filtering (typically with 200 or 400 Hz cutoff frequency). The envelope outputs are finally compressed using nonlinear compression function (e.g., logarithmic) to ensure that the envelope outputs fit the patient's dynamic range of electrically evoked hearing.

4. PERFORMANCE

MATLAB's Filter Design and Analysis tool (FDA Tool) is used to generate Band Pass FIR filter coefficients by using Hamming window of 128 orders. The magnitude response of the designed 8 band FIR filters as shown in Figure 7 with corresponding frequency bands in the Table 1.

Figure 6: Software Implementation of 8 Channel CIS Algorithm

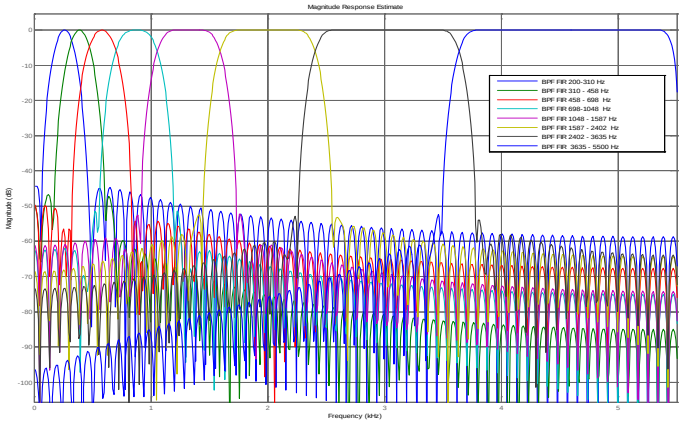


Figure 7: Magnitude Response of 8 Channel Band Pass Filter

Table 1: Filter Bands for 8-Channel CIS Algorithm.

Band Number	Frequency in Hz	Center Frequency In Hz
1	200-303	251
2	303 - 458	380
3	458 - 693	575
4	693 -1049	871
5	1049 -1587	1318
6	1587 -2402	2000
7	2402 -3635	3018
8	3635 -5500	4570

The fixed 8-channel CIS algorithm is modified in our work to suit to either 4-channel CIS or 5-channle CIS or 6-channel CIS or 7-channel or 8-channel operation with flexibility in programming n-channel CIS algorithm where n = 4, 5,6,7,8 that is highly needed based on selected number (4/5/6/7/8) of active electrode out of 12 electrodes of electrode array placed in cochlea [Frijns, 2003]. The CIS algorithm is validated by using various single tone frequency signals generated by using signal generator. The input and output signals are observed at various stages of implemented CIS algorithm by using FPGA in 8-channel Scope Coder measuring instrument. The designed system can be programmed to perform 4 to 8 channel CIS algorithm based on the number of active electrodes for speech/sound frequency range 200 to 5500Hz. The ADSP2185 can perform (i) 8 channel, (ii) 7 channel, (iii) 6 channel, (iv) 5 channel and (v) 4 channel CIS algorithm. The frequency distribution for 4 to 8 channel for the allowable frequency range is shown in Table 2.

A total of (8+7+6+5+5=31) FIR band pass filters are designed to perform the required functionality. All 32 FIR bandpass filter performance is tested for functionality using single tone frequency signal from signal generator to the speakers. The testing of FIR bandpass filters is done as follows. The frequency of the signal generator is set to the each bands center frequency. For example, 8 channels BPF, the function generator frequency is set at 610Hz and given to the line input of CODEC and each channel BPF FIR filter output is sent to the Line output of CODEC and the output response are observed. The Observed waveforms for the frequency of 610 Hz frequency it belongs to band 3. As only band 3 FIR filter allows the signal, the remaining Band Pass Filters attenuates the signal. The recorded waveform for the 3rd Channel BPF FIR Filter of 8-channel CIS algorithm as shown in Figure 8. Full-wave Rectification: After each band pass filtering has done, the filter waveform is rectified by using full wave rectification. Sample output of 3rd channel output after rectification as shown in Figure 9. After rectification again the processed sample is filtered by the 32 order low pass filter of 0-400Hz to extract the temporal information of each channel. Output of the LPF FIR filter output is shown in Figure 10. After low-pass filtering the processed sample is stored in the buffer.

Table2: Frequency Distribution of 200 – 5500 Hz Frequency for 4/5/6/7/8 Channel CIS Algorithm

	Channel numbers							
Number of active Channels	1st Band (Hz)	2nd Band (Hz)	3rd Band (Hz)	4th Band (Hz)	5th Band (Hz)	6th Band (Hz)	7th Band (Hz)	8th Band (Hz)
4	200 - 458	458 -1050	1050- 2400	2400- 5500				
5	200 - 388	388 – 753	753 – 1460	1460- 2835	2835- 5500			
6	200 - 347	347 - 604	604 – 1049	1049 – 822	1822 - 3166	3166 - 5500		
7	200- 321	321-516	516 - 828	828 – 1329	1329 - 2134	2134 - 3426	3426 - 5500	
8	200- 303	303 - 458	458 - 693	693 -1049	1049 - 1587	1587 - 2402	2402 - 3635	3635 - 5500

Figure 8: Input and Output Signals of Channel 3 FIR Band Pass Filter with Mono Tone Frequency of 610 Hz

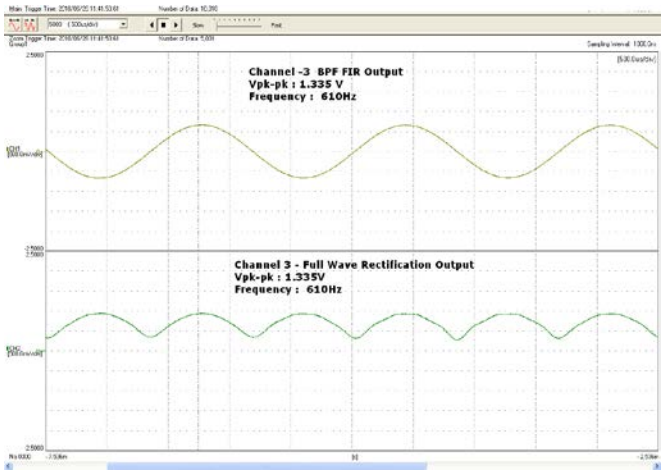


Figure 9: Input and Output Signals of Channel 3 Full Wave Rectifier

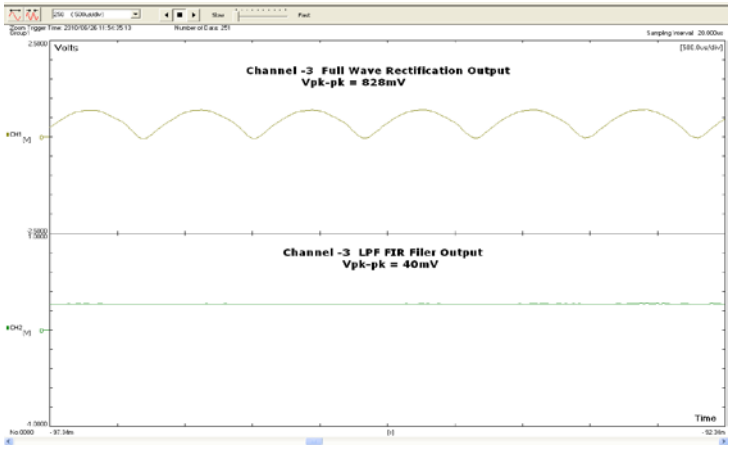


Figure 1: Input and Output Signals of Channel 3 FIR LPF Filter (0-400Hz).

After rectification again the processed sample is filtered by the 32 order low pass filter of 0-400Hz to extract the temporal information of each channel. Output of the LPF FIR filter output is shown in Figure 10. After low-pass filtering the processed sample is stored in the buffer.

5 . CONCLUSION

The Configuration of FPGA for speech/sound processing has been particularly use with Bio-computing systems. The flexibility and computational power of the developed system allows speech processing using CIS strategy, which is tested and evaluated. Speech processing schemes may be improved by including surrounding noise pollutions, increase the no of channels and speech intelligibility optimization.

6. ACKNOWLEDGEMENTS

The funding and technical support provided by NSTL, Visakhapatnam is acknowledged.

7.REFERENCES

[1] [Clark, 2006] Graeme M. Clark, "The multiple-channel cochlear implant: the interface between sound and the central nervous system for hearing, speech, and language in deaf people—a personal perspective", Phil. Trans. R. Soc. B , 2006, Vol. 361,pp 791–810

[2] [[Zeng 2004] Fan-Gang Zeng,"Trends in Cochlear Implants", Trends In Amplification, Volume 8, No. 1, 2004, pp T1-T34.

[3] [Hirshorn, 1986] Michael S . Hirshorn, Dianne J. Mecklenburg, Judith A. Brimacombe, "Nucleus 22-channel cochlear implant: Preliminary observations", Journal of Rehabilitation Research and Development, April 1986, Vol . 23, No . 2, pp 27-33.

[4] [Hmida, 2007] Ghazi Ben Hmida, Hamadi Ghariani and Mounir Samet , "Design of Wireless Power and Data Transmission Circuits for Implantable Biomicrosystem", Biotechnology, Asian Network for Scientific Information , Vol 6, no. 2, 2007, pp 153-164.

[5] [Hochmair, 2006], Ingeborg Hochmair, Peter Nopp, Claude Jolly, Marcus Schmidt, Hansjörg Schößer, Carolyn Garnham and Ilona Anderson, "MED-EL Cochlear Implants: State of the Art and a Glimpse Into the Future", Trends in Amplification , Vol. 10, No. 4, December 2006, pp 201-220.

[6] [Wilson, 2007], Blake S. Wilson and Michael F. Dorman, "The Surprising Performance of Present-Day Cochlear Implants", IEEE Transactions on Biomedical Engineering, vol. 54, no. 6,pp . 969-973, June 2007

[7] H. J. McDermott, "A programmable sound processor for advanced hearing aid research," IEEE Trans Rehab. Eng., vol. 6, pp. 53-59, March 1998.

[8] Chih-Kuo Liang, Gin-Shu Young, Jia-Jin Jason Chen* and Chung-Kai Chen, "Microcontroller-based implantable Neuromuscular stimulation system with Wireless power and data transmission for Animal experiments, Journal of the Chinese Institute of Engineers, Vol. 26, No. 4, pp. 493-501,2003

[9] G. A. Kendir, W. Liu, G. Wang, M. Sivaprakasam, R. Bashirullah, "An optimal design methodology for inductive power link with class-E amplifier," IEEE Trans. Circuits Syst.I, Reg. Papers, vol. 52, no. 5, pp. 857–866, May 2005

[10] HUGH McDERMOTT., "An Advanced Multiple Channel Cochlear Implant ", IEEE Trans Bio Medical Engg, vol 36 pp 787-797,July 1989

[11] Shannon, R., Zeng, F-G., Kamath, V., Wygonski, J. and Ekelid, M., "Speech recognition with primarily temporal cues," Science, Vol.270 ,p303-304. October 1995.

[12] B. S.Wilson, C. C. Finley, D. T. Lawson, R. D.Wolford, and M. Zerbi, "Design and evaluation of a continuous interleaved sampling (CIS) processing strategy for multichannel cochlear implants," J Rehabil. Res. Dev., vol. 30, no. 1, pp. 110–116, 1993.