A Simple Technique for Enhancing Conversion Speed of Successive Approximation ADC

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Abstract

High resolution analog to digital converters (ADC's) have been based on self–calibrated successive approximation technique, because it uses a single comparator and consumes less power. Unfortunately successive approximation technique requires N comparisons to convert N bit digital code from an analog sample. This makes successive approximation ADC's unsuitable for high speed applications. This paper demonstrates a simple technique to enhance speed of successive approximation ADC's that require as few as N-5 comparisons for N bit conversion. This technique optimizes the number of comparator requirements while increasing conversion speed by 62.5% for 8-bit resolution. In our approach, the analog input range is partitioned into 32 quantization cells, separated by 31 boundary points. A 5-bit binary code 00000 to 11111 is assigned to each cell. A normal successive approximation converter requires 8 comparisons for 8-bit quantization, while our proposed technique reduces number of comparison requirements to only 3 for 8 bit conversion. Therefore this technique is best suitable when high speed combined with high resolution is required. Result of 8-bit prototype is presented.

Keywords: *ADC, Microcontroller, DAC, Sample and Hold. Successive approximation.*

1. Introduction

Digital control systems are extensively used in the field of motion control. High performance digital control systems have created a need for high speed and high resolution analog to digital converters (ADC's) with extremely wide dynamic range. Typically high-resolution ADC's have been based either on self-calibrated successive approximation [1-3] or over sampling architectures [4, 5]. But both of these architectures are unsuitable for high speed applications. Two step Flash converters are popular for conversion resolutions in the 8-12 bit range where optimized designs can achieve low power dissipation and small silicon area for implementation [6, 7]. However, beyond such resolution, the area and power dissipation of two-step Flash ADC's nearly double for each additional bit of resolution [8].

There are many different architectures like pipelined convertor [9, 10], successive approximation convertor [11, 12], Sigma-Delta convertor [13], folding ADC's [14], reported recently for high speed applications. But these architectures have significant amount of complexity. In this paper a simple technique for enhancing conversion of successive approximation ADC is proposed.

2. ARCHITECTURE DESCRIPTION

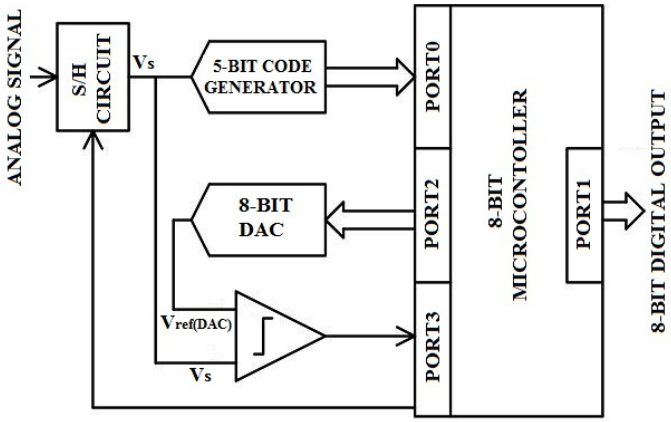

Figure 1 Block diagram of 8-bit ADC

A wide variety of successive approximation ADC architectures have been described by several authors [1-3]. Successive approximation ADC's are promising for low power, high resolution applications. However, high resolution limits the speed. The ADC based on our technique enjoys the benefit of employing only 29 comparators instead of 255 comparators normally required in conventional 8-bit Flash architecture while maintaining the advantage of high speed. In the proposed technique, segmentation process increases the speed of conversion. In such converters, it can be shown that quantization speed increases drastically. For example to achieve 8 bit resolution, with 5 bit first stage only three comparisons are required. The comparison requirement is drastically reduced than non segmented converters.

Table 1: Trade-off between number of comparisons and number of bits

Bits	**8**	**10**	**12**	**16**	**20**	**24**	**32**
4	4	6	8	12	16	20	28
5	3	5	7	11	15	19	27
6	2	4	6	10	14	18	26
7	1	3	5	9	13	17	25
8	0	2	4	8	12	16	24

The trade-off between number of comparisons required to complete conversion and number of bits in the first stage is summarized in Table 1, where 8 to 32 at the top row corresponding to ADC resolution in bits, 4 to 8 in the left column are corresponding to number of bits in the first stage. Although higher number of bits in the first stage decreases number of comparisons requirements, it increases complexity and power. Block diagram of the 8-bit ADC using proposed technique is illustrated in Figure 1. In the proposed technique**,** the analog input range is partitioned into 32 quantization cells, separated by 31 boundary points. **A** 5-bit binary code 00000 to 11111 is assigned to each cell**;** Table 2 summarizes Binary code and corresponding centre value of each cell. The proposed ADC consists of the sample and hold circuit (SHC), 29 comparators, 8-bit DAC, Microcontroller 8051. ADC is built by cascading a 5-bit code generator with 3-bit successive approximation ADC. Where 5-bit code generator works as first stage which decides within which cell the analog sample lies and produces 5-bit binary code corresponding to that cell. Second stage as successive approximation ADC this produces final 8-bit digital code.

Table 2: Binary code and centre value of cells

Cell No. (N)	Maximum Voltage of the cell(V_N)	Binary Code for the cell (B_N)	Mid Value Binary Code of the Cell (MB_N)
0	0.1094	00000	00000100
1	0.2188	00001	00001100
2	0.3282	00010	00010100
3	0.4376	00011	00011100
4	0.5470	00100	00100100
5	0.6564	00101	00101100
6	0.7658	00110	00110100
7	0.8752	00111	00111100
8	0.9846	01000	01000100
9	1.0940	01001	01001100
10	1.2034	01010	01010100
11	1.3128	01011	01011100
12	1.4222	01100	01100100
13	1.5316	01101	01101100
14	1.6410	01110	01110100
15	1.7504	01111	01111100
16	1.8596	10000	10000100
17	1.9692	10001	10001100
18	2.0786	10010	10010100
19	2.1880	10011	10011100
20	2.2974	10100	10100100
21	2.4068	10101	10101100
22	2.5162	10110	10110100
23	2.6256	10111	10111100
24	2.7350	11000	11000100
25	2.8444	11001	11001100
26	2.9538	11010	11010100
27	3.0632	11011	11011100
28	3.1726	11100	11100100
29	3.2820	11101	11101100
30	3.3914	11110	11110100
31	3.5008	11111	11111100

2.1 Five bit Code Generating Circuit

First stage of the proposed technique is simple rearrangement of the Flash architecture. The conventional 5-bit Flash quantizer uses 31 comparators [15], a 32:5 priority encoder. Whereas first stage of the proposed technique uses only 28 comparators, 8:3 priority encoder, this simplifies the circuit complexity. The decrease in the number of comparators and number of inputs in a digital encoder decreases the total area and power dissipation. The decrease in the number of comparator also decreases the capacitive load on sample and hold circuit. First stage circuit produces 5-bit code in three steps. A 3-bit Flash quantizer and a sample and hold circuit as shown in Figure 2, samples the analog input voltage and 3-bit digital code is generated in the first step. In second step, fourth bit is obtained by thermometer code generator and 8:1 Multiplexer as shown in Figure 3. Fifth bit is generated in third step, by multiplexing 14 lines of thermometer code generator onto a single data line as shown in Figure 4. Finally the 8-bit digital code is obtained by successive approximation method.

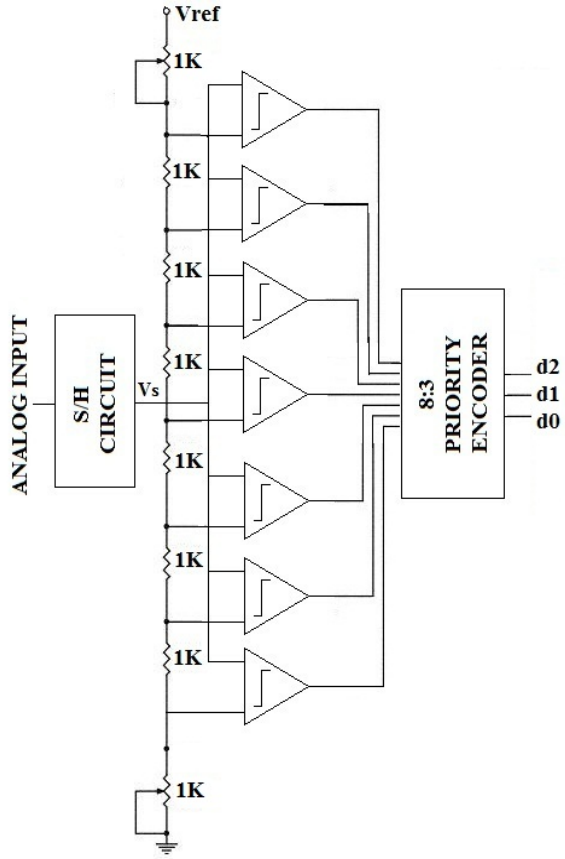

Figure 2 Three bit Flash Convertor

2.2 Successive Approximation method.

Second stage of the proposed technique is successive approximation ADC. The microcontroller 8051 reads 5-bit code from first stage and loads corresponding mid value code of a particular cell (MB_N) into the accumulator. The conversion algorithm is similar to the binary search algorithm. First, the reference voltage of a particular cell, $V_{ref\ (DAC)}$ provided by DAC is set to the $V_N / 2$ to obtain the MSB, where V_N is the maximum cell voltage of a particular cell and N is cell number. After getting the MSB, successive approximation convertor moves to the next bit with $V_N/4$ or $3/4*V_N$ depending on the result of the MSB. If the MSB is "1", then $V_{ref(DAC)} = ¾*V_N$, otherwise $V_{ref(DAC)} = V_N/4$. This sequence will continue until the LSB is obtained. Figure 5

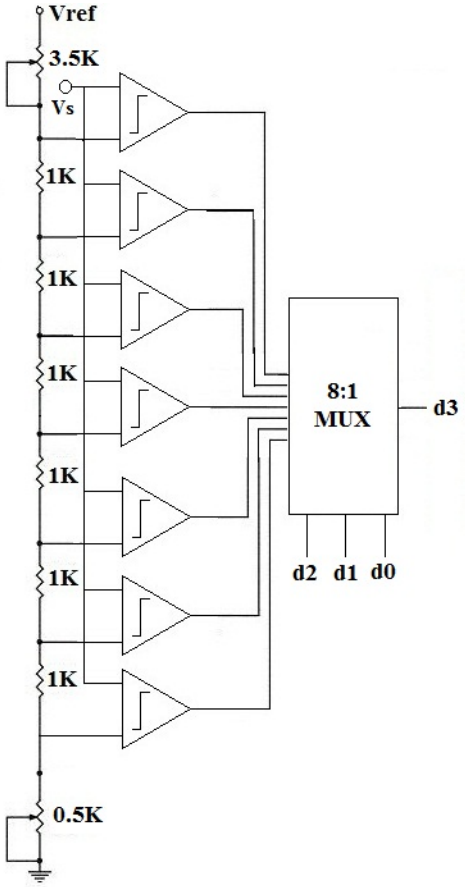

Figure 3 Bit d3 generating circuit

shows how the reference voltages are implemented for analog signal sample lies in the third cell. Note that $7/8*V_3$ is the largest reference voltage and $1/8*V_3$ is the smallest reference voltage. To get an 8-bit digital output, 3

comparisons are needed, while it is 8 comparisons in the normal successive approximation ADC.

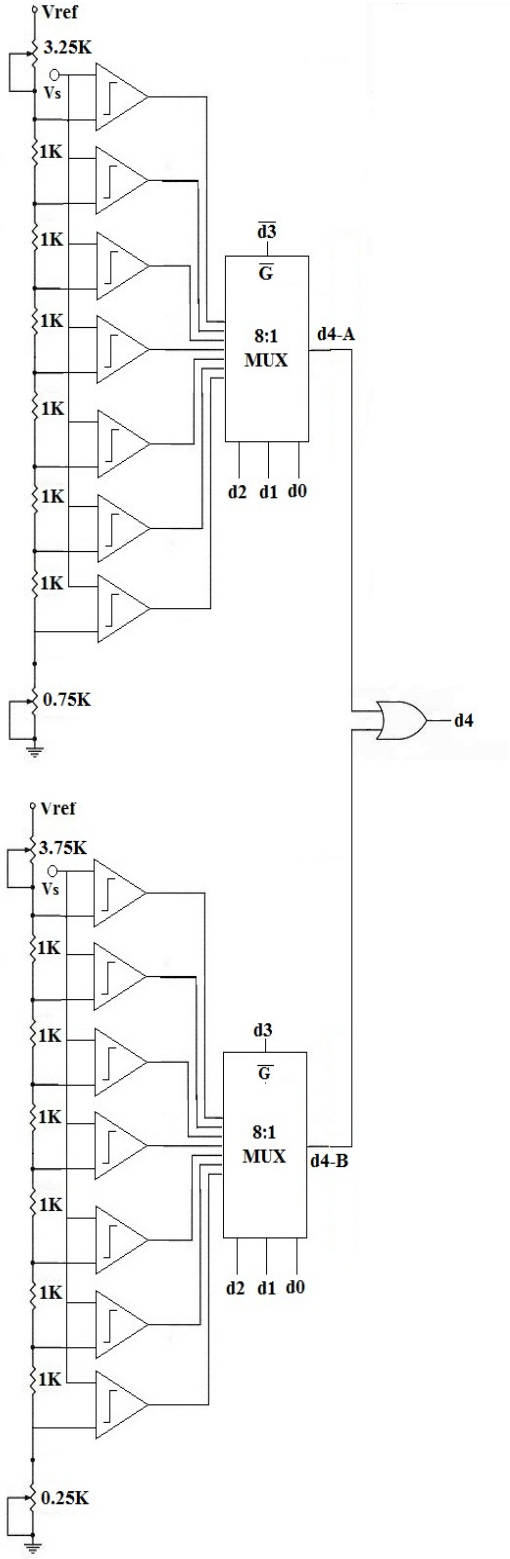

Figure 4 Bit d4 generating circuit

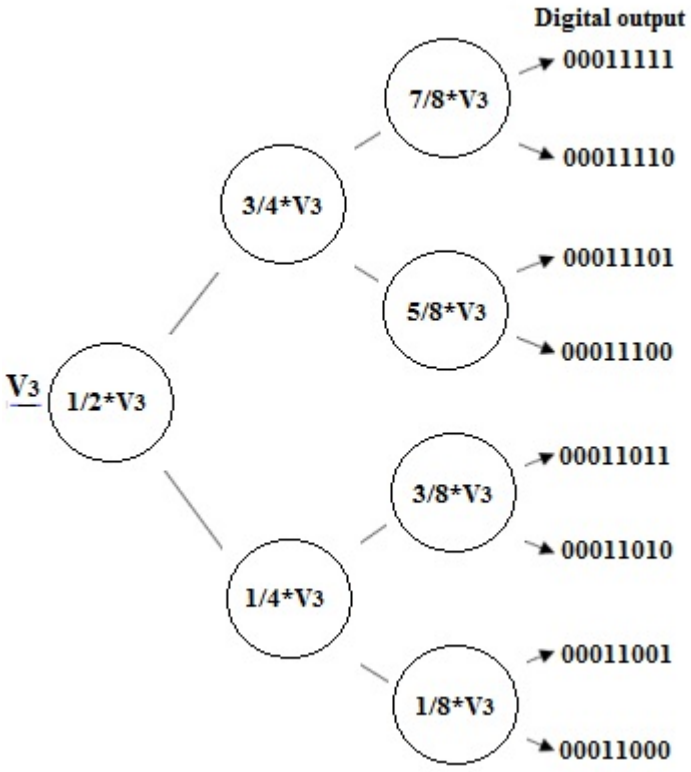

Figure 5 Reference voltage tree in successive approximation ADC

3. CIRCUIT DESCRIPTION

Proposed technique employs two stages for quantization of a given analog signal. The first stage 5-bit generating circuit processes the input analog signal in three steps. In the first step, illustrated in Figure 2, the analog input signal is sampled and quantization is performed by the three bit Flash quantizer. In the second step, shown in Figure 3, the fourth bit is obtained by thermometer code generator and 8:1 multiplexer. Each of the seven comparator of a thermometer code generator has a reference input voltage from a precision reference voltage source V_{ref}. A resistor string voltage divider network provides 0.05 V_{ref} in steps of 0.1 V_{ref}. The other input terminal of each comparator is driven by the sampled analog input voltage. An output condition of thermometer code generator is routed onto a single line using 8:1 multiplexer. Three MSB bits from Flash quantizer, determines which output of a comparator is to be routed.

Final bit of first stage is obtained in third step as shown in Figure 4, by ORing outputs of two 8:1 multiplexer. The fourteen comparator of thermometer code generator has a reference input voltage from voltage source V_{ref}. A resistive potential divider network provides 0.025 V_{ref} to

0.625 V_{ref} and 0.075 V_{ref} to 0.675 V_{ref} in steps of 0.1 V_{ref}. The other input terminal of each comparator is driven by the sampled input voltage. Fourteen output conditions of thermometer code generator are routed onto a single line using two 8:1 multiplexer. Three MSB bits from Flash quantizer and fourth bit from second step quantizer determine which output is to be routed.

In second stage, 8-bit digital code is obtained by successive approximation technique. As shown in Figure 1, port 1 of Microcontroller is used to read the 5-bit output code of first stage and a constant 3-bit binary code 100. This byte is loaded in register A. Port 3 is used to send start of conversion pulse and also to read status of DAC comparator. A digital-to-analog converter 0808 is connected to port2. Port2 furnishes the digital byte in the register A to a DAC. The digital code for an analog input signal is routed on to port 4.

Figure 1 indicates that only one comparator is needed for the second stage to yield the final 8-bit digital code, while another twenty eight comparators are used in the first stage total of twenty nine. This is much less than the 255 needed in a full-Flash 8-bit ADC.

Software for implementing successive approximation converter in Microcontroller is written in assembler code and converted to hex code by assembler software. Hex codes are transferred to microcontroller by programmer. Flowchart of software is shown in Figure 6.

4. MEASURED RESULT

An experimental prototype of 8-bit ADC using proposed technique was designed and developed using Philips P89V51RD2BN. The working functionality of the ADC has been checked by generating a ramp input going from 0 to 3.5V (full scale range of the ADC). Digital codes have been obtained correctly, going from 0 to 255 for 8-bit at the output, indicating that the ADC's working is functionally correct. Results are depicted in Figure 7.

Both the differential and integral nonlinearities (DNL and INL) were measured over 2^8 output codes by applying slowly varying full scale range ramp as input to the proposed ADC, which completes the full scale range in 255 steps .The values of the each code are compared with ideal value and store the difference value. The results show that the ADC exhibits a maximum DNL of 0.47LSB and a maximum INL of 0.5LSB as shown in the Figures 8(a) and 8(b).

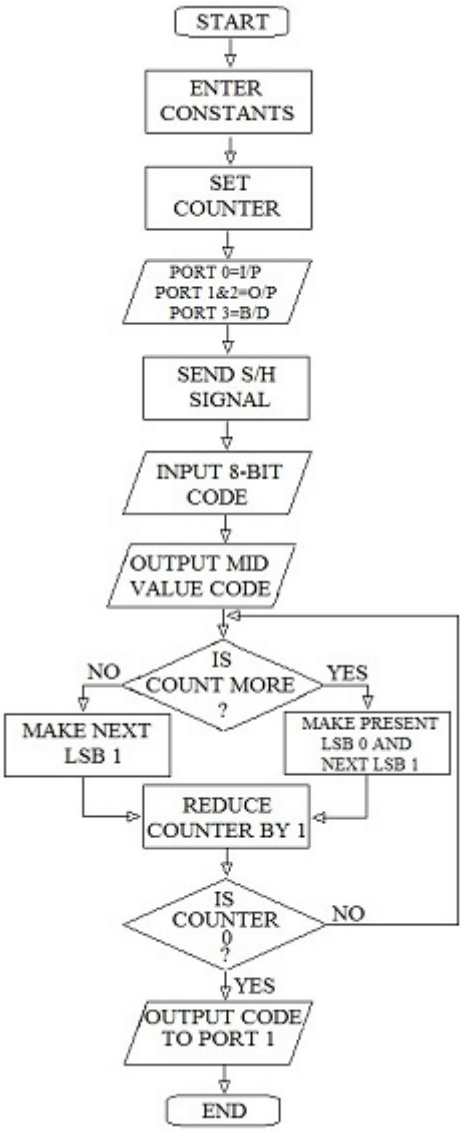

Figure 6 Flowchart of software

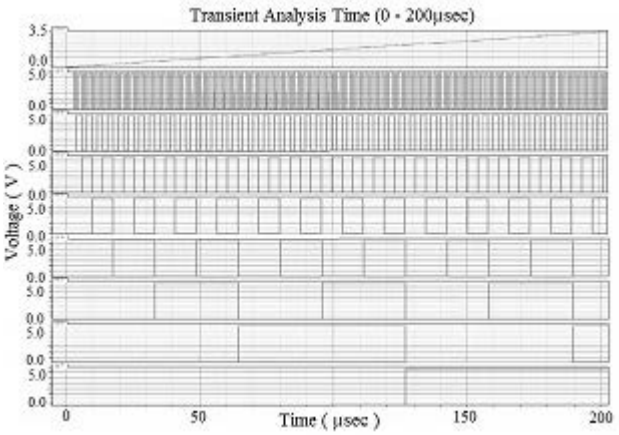

Figure 7 Transient Analysis of 8-bit ADC

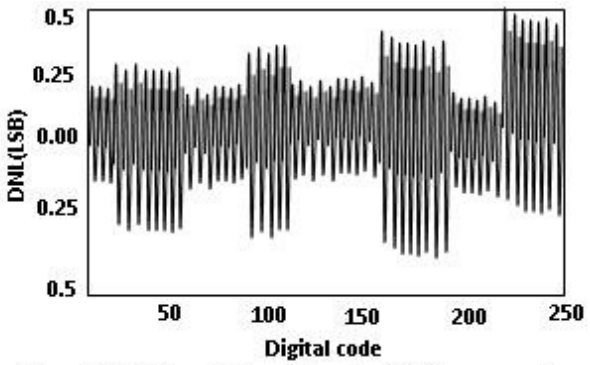

Figure 8(a) Differential Non Linearity Versus output Code

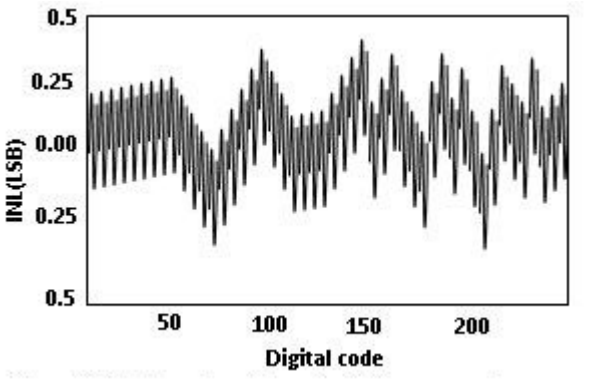

Figure 8(b) Integral Non Linearity Versus output Code

5. CONCLUSION

We have presented a simple and effective technique for enhancing speed of a successive approximation ADC. This technique would be effective in a large number of high speed controls and signal processing applications such as hard-disk-drive read Chanel and wireless receivers. Although these applications are most often implemented with Flash convertors, but these ADC's demands larger power. Also, the ADC die area and power dissipation increase exponentially with resolution, limiting the resolution of such ADC's less than 10bits. This paper shows that partitioning analog input range increases the conversion rate of successive approximation ADC's. The main conclusion is that although Flash convertors provide high conversion rates, required power dissipation of these ADC's are large. Also, resolution beyond 10bits these ADC's become prohibitively expensive and bulky. Proposed technique provides high enough conversion speed for high speed applications, with less power dissipation even beyond 10bit resolution. Implementation of successive approximation algorithm in Microcontroller has reduced the hardware requirement and cost. Proposed technique uses only 29 comparators to enhance speed of 8-bit successive approximation ADC by 62.5%.

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