A Novel Seven Input Majority Gate in Quantum-dot Cellular Automata

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Abstract

A Quantum Cellular Automaton (QCA) is a nanotechnology which is an attractive alternative for transistor based technologies in the near future. A new seven input majority gate in quantum dot cellular automata is proposed in this paper. The basic elements in QCA are majority and inverter gates, therefore using a majority gate with more inputs in QCA circuit will cause reduction in cell count, latency and complexity. Furthermore, by using the proposed seven input majority gate we can design four inputs AND gate and OR gate in only two clock phases. By applying these kinds of gates QCA circuits could be simplified and optimized. In order to prove the functionality of the proposed device, QCADesigner tool and some physical proofs are utilized.

Keywords: *Quantum-Dot Cellular Automata, Majority gate, AND gate, OR gate, Nanoelectronic circuits.*

1. Introduction

CMOS technology has experienced serious problems such as short channel effects, doping fluctuations, increasingly difficult and expensive lithography at nano scale, high leakage current and speed limitation in GHz range. Many alternative technologies have been introduced in the Industry Technology Roadmap for Semiconductors (ITRS) [1]. A Quantum-dot cellular automaton (QCA) is one of these promising nanotechnologies that could be utilized instead of conventional transistor technology in the future.
Quantum-dot Cellular Automata provides new possibilities to achieve outstanding properties such as extremely high density and fast operation speed at Tera Hertz frequencies together with low power dissipation [2-4].
QCA circuits are implemented with two principle gates: majority and inverter gates. As the basic element in QCA is majority gate, the structure of this gate is a significant factor in designing circuits in QCA [5-7]. The very recent designs have been constructed with three input majority gate [8-11]. Although these designs work correctly, they can be reconstructed using new devices to reduce cell counts, clock phases and complexity. Recently five pins majority gates with a new compact full adder cell with lower area and cell counts have been proposed in [12-15].
This paper investigates novel 7-input majority design in QCA. This proposed design only works in two clock phases and in one layer. The input and output of this proposed design is located in two separate sides representing a powerful advantage for designing QCA circuit. By applying this form of majority gate we can simplify logical functions and achieve improved results.
The rest of this paper is organized as follows: in section 2, a brief review of QCA technology is provided and the implementation of the novel seven input majority gate is proposed in section 3. Then accuracy of the proposed design is verified by using physical relations. Finally, in section 4 simulation results are demonstrated and conclusions are drawn in section 5.

2. Review of QCA

In this section we propose a brief background of basic elements of QCA. The basic element of QCA is a cell. A QCA cell, shown in Fig 1, due to the Columbic interactions consists of four quantum dots at the corners of a square with two extra mobile electrons in two different configurations, thus we have two polarizations (p= +1 , p= -1) used for encoding binary information [5][16-17].

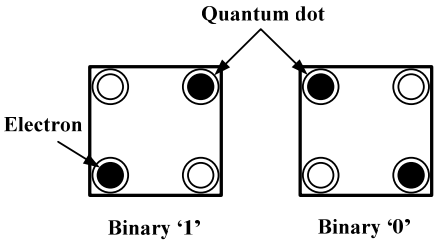


Fig. 1 Basic QCA cell and two possible polarizations

The Columbic interactions between two neighbor cells cause these cells to have the same polarizations. Therefore a series of QCA cells performs as wire in QCA (Fig 2) [18-19].

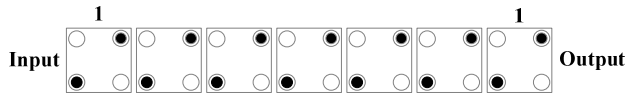


Fig. 2 A QCA Wire

The principle QCA logical circuits are majority and inverter gates. Fig 3 demonstrates two different inverter gates that were presented in [6].

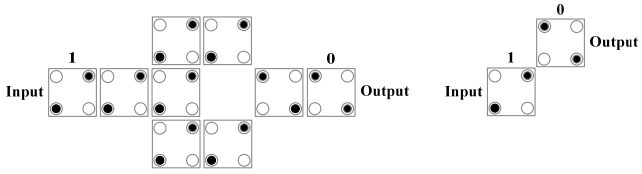


Fig. 3 QCA inverter gates

Up to now, most circuits have been implemented by three majority gate that act based on Eq. (1) (Fig 4) [7-9][20]. Recently a five input majority gates have been presented in [13-14]. Functionality of a five input Majority gate is shown in Eq. (2) and its QCA implementation is presented in Fig 5.

$$M(A,B,C)=AB+AC+BC \quad (1)$$

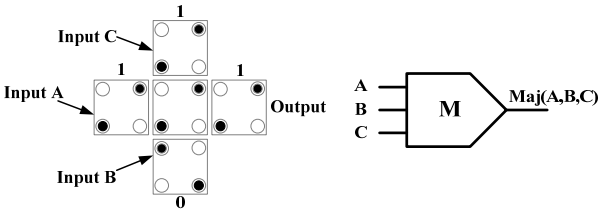


Fig. 4 A QCA three-input Majority voter

$$M(A,B,C,D,E)= ABC + ABD+ ABE+ ACD+ ACE+ ADE+ BCD+ BCE+ BDE+ CDE \quad (2)$$

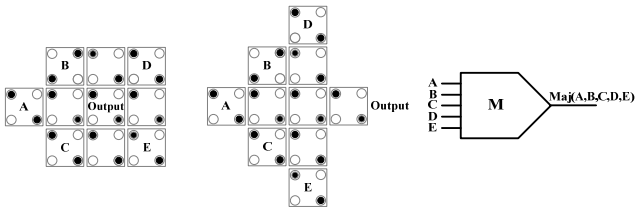


Fig. 5 Structures of Five-input Majority gates[13-14]

3. Proposed seven input Majority Gate

3.1 Design of novel seven input majority gate

A seven input majority gate comprises of seven inputs and one output. The design of this gate is based on five majority gate that was proposed in [14]. A truth table of the seven input majority gate based on sum of inputs is shown in Table 1 and the QCA implementation of majority voter can be presented as Fig 6.

Table 1: Truth table of seven-input majority gate based on sum of inputs

∑(A,B,C,D,E,F,G)	M(A,B,C,D,E,F,G)
0	0
1	0
2	0
3	0
4	1
5	1
6	1
7	1

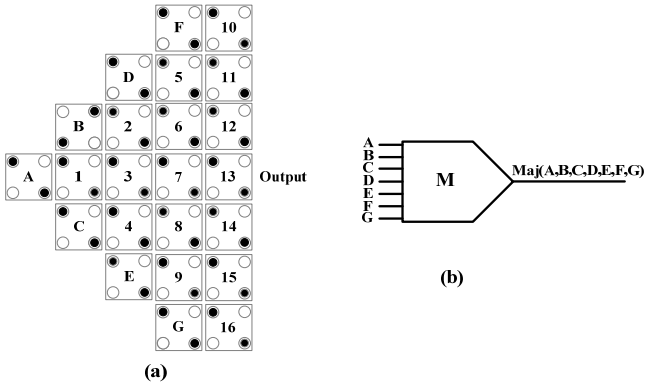


Fig. 6 (a) Proposed seven input majority gate (b) Schematic symbol for the majority gate

In this scheme, labels *A, B, C, D, E, F* and *G* are inputs and the output cell is shown by *output*. Middle cells labeled 1 through 16 are device cells and these middle cells are affected by neighbor cells (input cells or other middle cells). Through these effects, the majority decision

of inputs is transferred to the output and efficiently constructs the seven-input majority gate.
By using this device and fixing three inputs, we can implement four input AND gate and four input OR gate, which can reduce the complexity, area and latency of the complex QCA circuits instead of using conventional three input majority gates. Functionality of these gates is presented in Eq. (3a) and (3b).

$M(A,B,C,D,0,0,0)=ABCD$ (3a)
$M(A,B,C,D,1,1,1)=A+B+C+D$ (3b)

The schematic symbols of four input AND and four input OR gates are illustrated in Fig 7. In order to illustrate the usefulness of this type of gates, some logical functions such as XOR, MUX and compressor should be simplified.

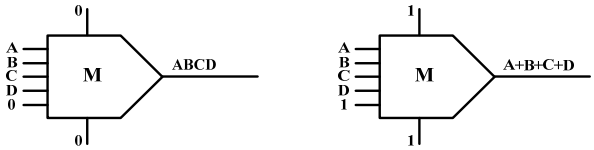


Fig. 7 schematic symbol of four input AND gate and four input OR gate.

3.2. Physical proof:

For physical proof, we assume that all cells are similar, the length of each one is (*a=18nm*), there is a space of x (*x=2nm*) between each two neighbor cells and only neighbor cells would affect each other.
It should be noted that in order to achieve more stability, electrons of QCA cell are arranged in such a manner that their potential energy reaches the minimum level. The potential energy between two cells is calculated using Eq. (4). In this equation, U is potential energy, k is fixed colon, q_1 and q_2 are electric charges and r is the distance between two electric charges. U_T is the summation of potential energies between two cells [21-23].

$$U = \frac{kq_1q_2}{r} \quad (4a)$$

$$kq_1q_2 = 9*10^9*(1.6)^2*10^{-38} = 23.04*10^{-29} = A = cte$$

$$U_T = \sum_{i=1}^{4} U_i \quad (4b)$$

As an example, the potential energy of neighbor cells (Fig 8) as well as other states can be calculated.
The Table 2 illustrates the computation results of potential energies for other states.

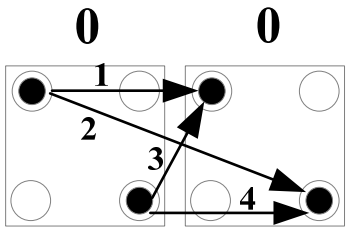


Fig. 8 A sample for computation of potential energy

$$U_1 = \frac{A}{r_1} = \frac{23.04*10^{-29}}{20*10^{-9}} \approx 1.152*10^{-20}(J)$$

$$U_2 = \frac{A}{r_2} = \frac{23.04*10^{-29}}{41.59*10^{-9}} \approx 0.553*10^{-20}(J)$$

$$U_3 = \frac{A}{r_3} = \frac{23.04*10^{-29}}{18.11*10^{-9}} \approx 1.272*10^{-20}(J)$$

$$U_4 = \frac{A}{r_4} = \frac{23.04*10^{-29}}{20*10^{-9}} \approx 1.152*10^{-20}(J)$$

$$U_T = 4.129*10^{-20}(J)$$

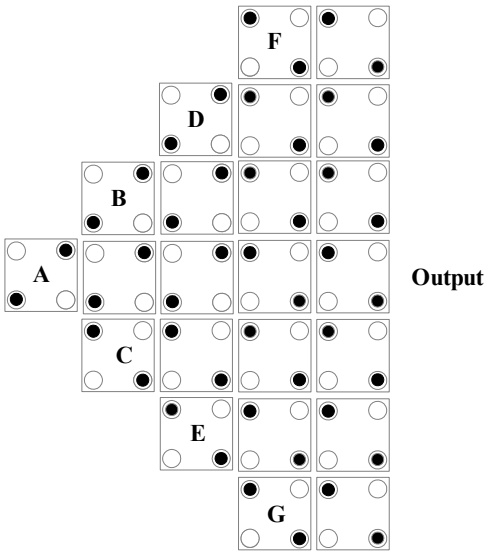
As in the above method, we can calculate the potential energy of all 128 different input states in seven majority gate to verify the accuracy of functionality. Here, two possible states (Fig 9) are proved.
In Fig 9(a), the input states are fixed (A=1, B= 1, C=0, D=1, E=0, F=0, G=0) and the value of the 16 device cells are computed in 2^16 possible states. First, we calculate the total potential energy with fixed zero value of device cells due to Table 2. In a similar manner, the total potential energy of other possible state of device cells can be simultaneously computed. The comparison of total potential energies in all states determines which state is more stable. The state which has the lower potential energy level is more suitable. According to computation results of potential energy, minimum energy achieved is $367.461*10^{-20}(J)$ when the value of output is zero. Similarly, the minimum total potential energy of input states (A=0, B=1, C=1, D=0, E=1, F=1, G=0) can be obtained as in Fig 9(b).
According to the above computing, the proposed structure for implementing seven input majority gate works accurately as the majority voter.
Further to physical proof, we can also check the proposed design using QCADesigner. Simulation of this majority gate is shown in the next section.

Table 2: The computation results of potential energies.

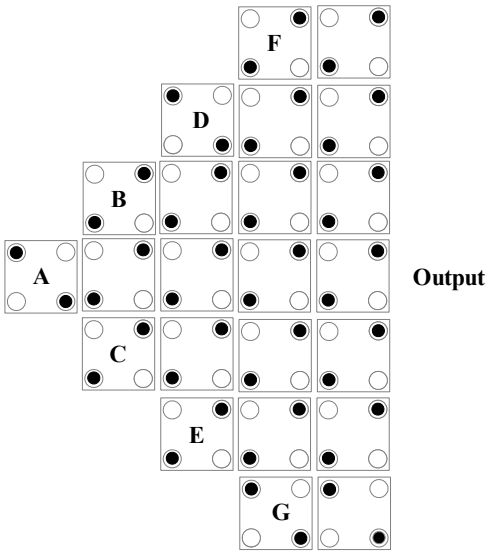
$*10^{-20}(J)$			
0 0	4.129	0 1	13.838
1 0	13.838	1 1	4.129
0 0	10.226	0 1	3.364
0 1	3.364	1 1	2.838
0 0	2.838	0 1	3.364
1 0	3.364	1 1	10.226
0 0	4.129	1 0	13.838
0 1	13.838	1 1	4.129

4. Simulation Results

The proposed seven input majority gate is implemented and simulated using QCADesigner version 2.0.3 [24]. The following parameters are used for a coherence vector options: cell size = 18nm, temperature= 1.000000 K, relaxation time= 1.000000e-015 s, time step= 1.000000e-016 s, total simulation= 7.000000e-011 s, clock high= 9.800000e-022 J, clock low = 3.800000e-023 J, clock shift = 0, clock amplitude factor = 2.000000, radius of effect = 80.000000 nm, relative permittivity = 12.900000, layer separation = 11.500000 nm. Most of the above mentioned parameters are default values in QCADesigner.



(a) Minimum Energy = 367.461* 10^{-20}(J)



(b) Minimum Energy = 359.547* 10^{-20}(J)

Fig. 9 Two possible states

The simulation result of new seven input majority gate is presented in Fig 10. For proving truth functionality of four input AND gate and OR gate, Figs 11 and 12 show the simulation results of these gates.

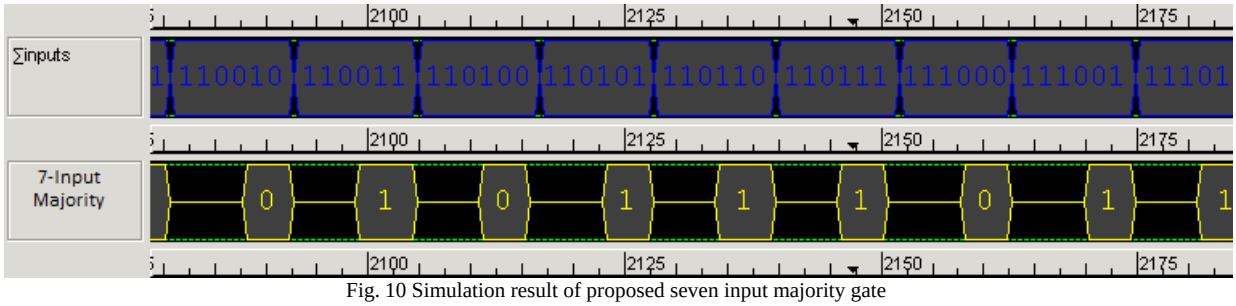


Fig. 10 Simulation result of proposed seven input majority gate

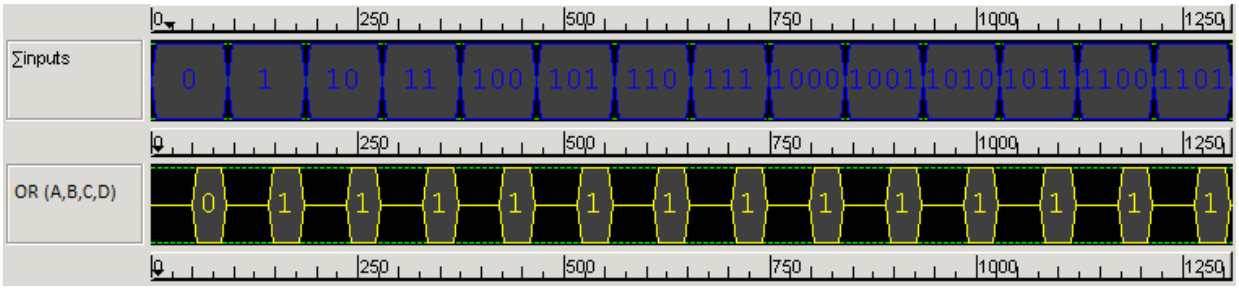


Fig. 11 Simulation result of proposed OR gate

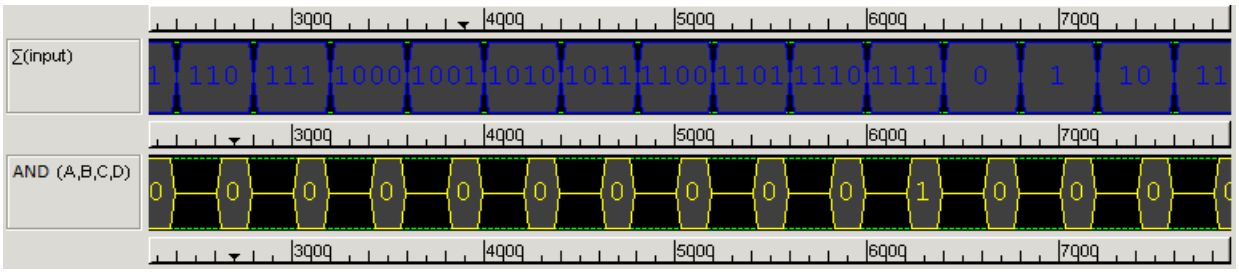


Fig. 12 Simulation result of proposed AND gate

5. Conclusion

A novel seven input majority gate for Quantum-Dot Cellular Automata is presented. For verifying the functionality, this proposed majority gate has been proved using physical relations and also verified in QCADesigner tools. By utilizing this seven input majority gate four input AND gate and OR gate can be achieved. Therefore most recent proposed designs in QCA can be simplified by using this majority device in order to reduce complexity, cell count and latency.

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