High Performance Charge Pump Phase-Locked Loop with Low Current Mismatch

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Abstract

In CMOS CPs, which have Up and Down switches made of p-channel and n-channel respectively, generates fluctuations in the VCO due to current mismatch occurs when dumping the charge to the loop filter and subsequently a large phase noise on the PLL output. This paper presents a new CP circuit after detailed analysis of the current mismatch problem. It combines an error amplifier with reference current sources to achieve good current matching characteristics and lower phase noises. Charge sharing can be eliminated by using charge removal transistors. In addition, a low-voltage cascode current mirror and gain-boosting circuit are used to enhance current matching over process corners and increase the output impedance of the CP. Good current matching characteristic is achieved with less than 0.1% difference of the Up/Down current and 1% over all process variations. The CP output compliance voltage range of 0.1-1.8 V is achieved for 1.8-V supply voltage. The circuit was designed using 0.18um TSMC CMOS technology and simulated by Spectre tools.

Keywords: *Charge pump (CP), gain-boosting charge pump, Voltage Controlled Oscillator (VCO) low-voltage cascode current mirror, phase-locked loop (PLL).*

1. Introduction

Since the conception of phase locking was proposed in the Thirties of the 20th Century, it has been widely applied in electronics and communication fields[1], especially used in large scale digital circuits. CP-PLLs (Charge Pump Phase-Locked Loop) are mainly used to generate signals and renew the clock pulses during the data transmission with high speed [5] [6]. As a key model, the charge pump plays an important role in assuring PLLs stability. It converts the digital signals in PFDs (Phase Frequency Detector) into analog signals of VCOs (Voltage Controlled Oscillator). When the phase-locked loop was locked in a certain frequency, the output voltage of charge pump is demanded to be a fixed value, and any tiny change of which will result in apparent frequency offset. Therefore, it is very important to design a charge pump circuit which can send a stable output voltage in CP-PLLs plan.

Phase-locked loops are widely used in clock generators and RF transceivers to ensure the accuracy of the oscillator frequency. The charge pump (CP) is an essential block in phase-locked loops (PLL). The CP consists of two switched current sources. Any current mismatch between the two current sources (i.e., difference between the source and the sink currents) would cause ripples on the control voltage. Ripples result in large phase noise and would also cause spurs on the PLL output signal [2].

This paper proposes a modified technique to decrease current mismatch in CP's using gain-boosting in addition to low-voltage cascode current mirrors [1]. Section II reviews the basic idea of the CP and the reasons behind current mismatch. Section III and IV deals with Charge sharing problem and current matching characteristics respectively. Section V introduces the proposed circuit architecture. Finally simulation results and comparisons in section VI. Section VII concludes the paper.

2. Basic Principle

Fig. 1 shows the circuit diagram of a conventional charge pump. In the charge pump, the digital output signals (UP and DN) of the PFD control the two circuit sources (IUP and IDN), and charge the capacitance CL via two switches which generally substituted by two MOSFET to obtain the DC level Vctrl needed by the Voltage Controlled Oscillator.

In Fig.1 the IUP and IDN should be completely equal in theory, but there are many nonideal effects which will result in their

mismatching in practice [4]. Another ubiquitous problem is the charge sharing in conventional charge pumps which results from the parasitic capacitance of node A and B. The level in node A will be charged to VDD, and in node B be discharged to GND when the signal UP and DN are invalid, whereas the node A level will be falling and the node B level will be rising when the signal UP and DN are valid. The difference between Vctrl and node A will not be uniform to the difference between Vctrl and node B, thus bring on the charge redistribution among CL, A and B. Because the Ids will change with Vds, current source IUP or IDN will share the charge. It will result in current mismatch which make Vctrl jittering, and influence the circuit performance. The output Vctrl would be held if the charge and discharge current are well matched. Generally, the net current generated by the charge pump is not equal to zero because of the current mismatching, it will make the Vctrl increase a fixed value in every phase comparing time. The control voltage Vctrl should be held in an average value to maintain the loop in a locked status (as shown in Fig. 2(a)), then the phase-locked loop shall bring on phase error which make the net current of the charge pump be zero in every period, as shown in Fig. 2(b) where A1 and A2 have the equal area.

The phase error resulted from the current mismatch can be expressed as the following formula where Δton, Icp and |IUP- IDN| respectively represent the dead zone time of the PFD, the period of the reference clock, and the offset between CP current and charge, discharge current.

The eq.(1) indicates that, to lower the phase error, the dead zone time Δton and mismatch current |IUP-IDN| should be reduced, but the CP current Icp should be increased while the reference clock period is fixed. Holding a definite dead zone time will be propitious to overcoming the PFD dead zone, and the higher current Icp will increase the power consumption and noise, so lessening the mismatch current |IUP-IDN| is the key to lower the CP phase error.

2.1. Charge Sharing Problem

For the charge pump in Fig. 3(a) (Type A), charge sharing is caused by the parasitic capacitance in nodes *pcs* and *ncs* [7]. When I_{UP} is active, node *pcs* is charged to V_{DD} When deactivating I_{UP} some of the charge stored in node *pcs* will leak through the current source device. Since the parasitic of nodes *ncs* and *pcs* can never be matched, this will lead to a static phase offset. This is the transfer function of a phase-frequency detector followed by a Type A charge pump. The two transistors Mp and Mn in the Type B charge pump in Fig. 3(b) will remove the charge from the nodes *pcs* and *ncs* when Up and Down are deactivated [8].This leads to a large reduction in the phase offset.

Fig:2. Jitter transfer functions for different division ratios. (a) Simulated standard PLL. (b) Measured characteristics of Loop A with intentionally low damping.

Through the Mp device to the output when the Down control is inactive. When NMOS devices are used for speed-regulating the VCO, Vvco will never drop below Vtn, constraining Vqbn to be less than 2 Vtn which can easily be fulfilled. However, the charge pump works only up to an output voltage of Vvco< Vqbp + Vtp, limiting the upper tuning range of the VCO. However, the charge pump in Fig. 3(a) has the same upper voltage limit. Mismatch in I_{UP} and I_{DOWN} is a similar source of jitter as charge sharing described above. For low jitter, it is essential to have good matching, implying that the devices controlled by Vqbn/Vqbp should be saturated. Again, this requires Vvco< Vqbp + Vtp.

Charge removal can also be done by ac coupling [9], but this requires careful timing of the control signals in the charge pump. The solution to charge sharing in [10] is less suitable for low-applications due to the common-mode restrictions on the differential amplifier.

2.2. Current Matching Characteristics

Current matching characteristics is achieved by using an error amplifier as shown in Fig.4,, the voltage Vref, at the node REF of the current mirror *(M5* - Ms) follows the voltage *Vcpout* at the node CPOUT of the charge pump (M1~ *M4).* As a result, the voltage *Vref,* is equal to the voltage *Vcpout* as long as the amplifier maintains a high enough gain. For *M5* = M1, *M6* = *M2, M7* = M3 and M8 = *M4,* if the DOWN and the *UP* signal are high, then I4 = *I3* = *I2,* and if the DOWN and the UP' signal are low, then I3 = *I2* = I1. So we can make the sinking current *I4* equal the sourcing current Il. In this way, one can achieve nearly perfect source/sinking current matching characteristics regardless of the charge pump output voltages.

The proposed novel charge pump circuit which use error amplifier and reference current source to obtain the improved characteristic for

current match, and reduce the PLL's phase noise. Simultaneously, the charge sharing is effectively restrained by using charge removal transistors. So the circuit possesses good current match and high working speed. Current mirrors are then used to copy currents from the bias cell, and a cascode is used at the output node to get high output impedance in order to reduce current mismatch.

By using the gain-boosting technique, shown in Fig.5, high output impedance can be achieved without adding more cascode devices [1]. Gain-boosting saves some voltage headroom; this is significant for short channel length technologies, which have low supply voltage.

2.3 Proposed Circuit

The proposed CP circuit greatly improved the circuit performance by enhancing the current match and lessening the charge sharing, and at the same time, possessed the characteristics of high operating speed and low power consumption. In Fig.5, capacitance C1, C2 fill the role of stabilizing the node E and F's voltage to avoid instantaneous grid voltage fluctuation of the current source. The voltage Vc in node C will change with Vctrl by inserting an error amplifier which has the gain high enough to make Vc equal Vctrl. Moreover, M11 is designed to equal M9, M8 equal M10, M3 equal M5, and M4 equal M6, so the current I4 will be the same as I3, I1 when UP, DN level is holding high, and I2 will be the same as I1, I3 when UP, DN level is holding low.

Finally the current I4 equals I2, which lead up to the result of almost perfect drain-source current matching. M7 and M12 are named as charge eliminating transistor. When the transistors transfer from saturation to cutoff, the charge resting on the channel will be emitted to the source, and that the drain will not be impacted. When the UP and DN is low, the spare charge will be removed from node A and B, so that the charge sharing can be successfully restrained.

The proposed CP circuit which use error amplifier and reference current source to get good match characteristic, and use charge removal transistor to restrain the charge sharing. All the design has been simulated with Spectre tools.

The shortcoming of the structure is that it will confine the dynamic range, but it is not important in most situations. While Vctrl less than Vg5-Vtn and DN invalid, the current will move to the output via M7. The Vctrl will not be less than Vtn during NMOS used as VCO current control, and forcing the Vg5 less than 2Vtn will be easy to implement. Because the Vctrl is up to Vg10+|Vtp|, it restricts the Vctrl range. Transistor M7 and M12 also improve the switch speed of current, and supply DC level for node A, B while switch is turned off, which will prevent the pending nodes influencing the control Voltage.

A modification for the gain-boosting CP is illustrated in Fig.5, in which the channel length modulation problem is solved as well as current mismatch. A low voltage cascode current mirror is used to copy *IUp* and *IDown* from a single current source to ensure that both currents are equal. Fig.5.shows the low-voltage cascode current mirror. This current mirror is chosen because it provides high output impedance, and low channel length modulation mismatch [1].

As shown in Fig.5, the UpB and Down controlled switches have been embedded in the low-voltage cascade current mirrors, where M7 and M8 are the UpB and Down controlled switches respectively, M9 to M16 are the lowvoltage cascode current mirror transistors, and finally M17 and M18 are the reference current generators. The bias voltage of the low-voltage cascode current mirrors is chosen to be GND for the PMOS switched mirror, and VDD for the NMOS switched mirror, as these are the values of UpB and Down signals at lock. This provides better matching.

The output impedance, *Rout*, is higher than that given in Eqn**(2)**, since there is another cascode transistor, *Rout* is given by

$$Rout = R_{06}.gm_5.R_{05} \text{ at the node D.} \quad \text{----- (2)}$$

This value is large, and so large length transistors are not needed for having high output impedance.

2.4 Simulation Results

The proposed charge pump circuit, at the 1.8V power source, is simulated with Spectre tools. Fig.6. shows the simulation result of CP charge circuit, and Fig.7 -11 shows the stability, gain of VCO output and the charge pump current with reference and feedback signal. The graph has been plotted for both conventional and proposed charge pump PLL. The maximum difference of the Up/Down current is less than 0.1%. The proposed modified gain-boosting CP is designed using 1.8V CMOS transistors, good current matching is observed in addition to a wide compliance voltage range of 0.1-1.7 V**,** which relaxes the VCO design. The maximum value for the current mismatch is less than 0.1%. Current mismatch result of proposed CP and gain boosting CP is shown in table 1. The proposed design shows the highest gain and more stability.

3. Tables, Figures and Equations

3.1 Tables and Figures

Proposed Charge Pump		Gain Boosting CP	
Ip(μA)	Mismatch()	Ip(μA)	Mismatch()
16.23	0.61	14.5	0.8

Table 1: Current mismatch results

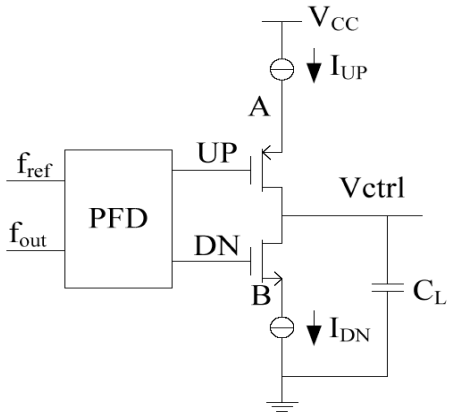

Figure.1 conventional charge pump schematic

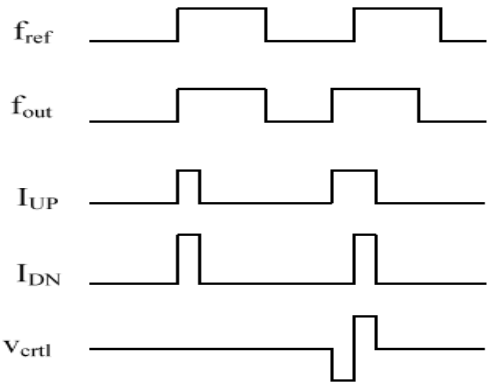

Figure 2(a): Charge and discharge current mismatch

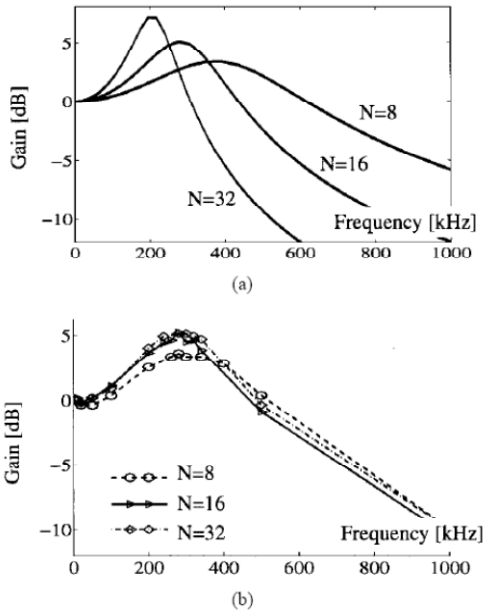

Figure 2(b): Jitter transfer functions for different division ratios. a) Simulated standard PLL. (b) Measured characteristics of Loop A with intentionally low damping

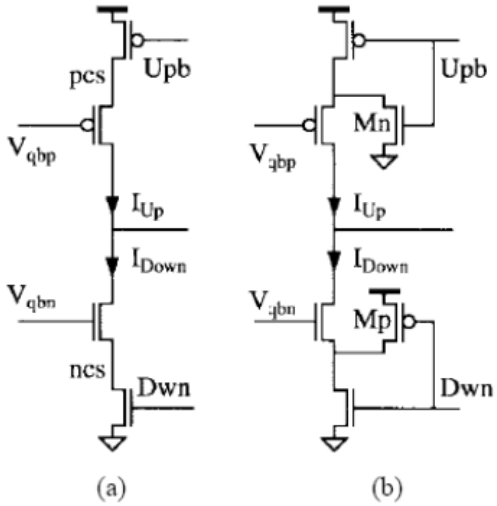

Figure 3: (a) Charge-pump suffering from charge sharing (Type A). (b) Charge removal transistors eliminate charge sharing (Type B).

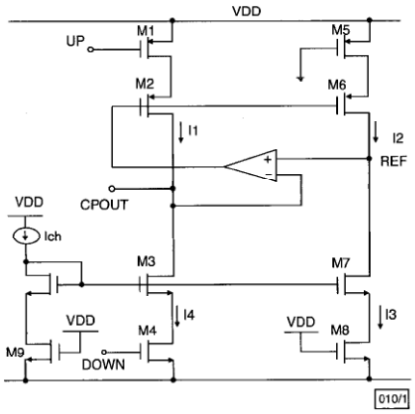

Figure 4: Charge pump circuit with good current matching

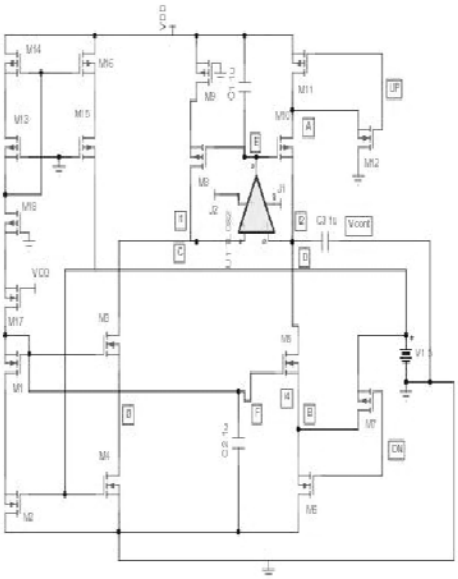

Figure 5: Proposed CP circuit

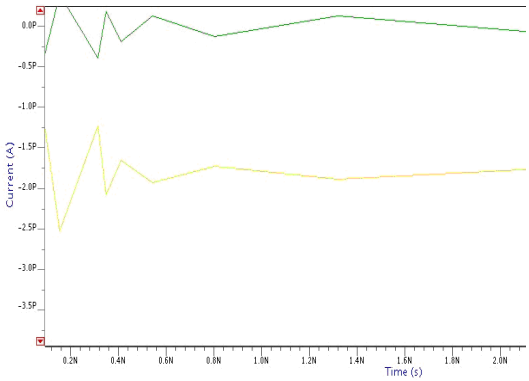

Figure 6: IUp and IDown currents Plots

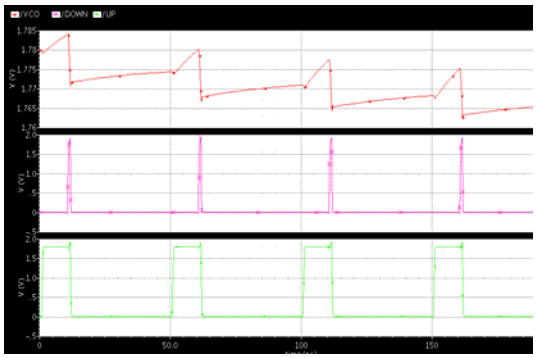

Figure 7: VCO control voltage when reference signal leads feedback signal (Conventional Charge Pump PLL)

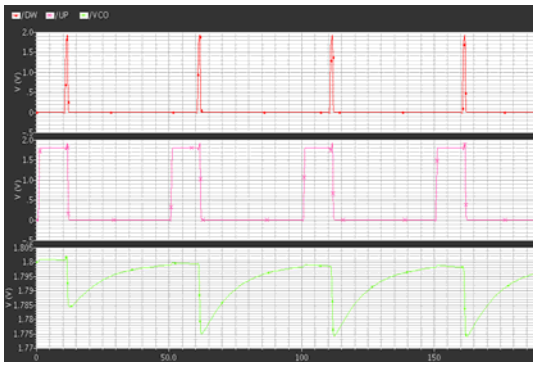

Figure 8: VCO control voltage when reference signal leads feedback signal (Proposed Charge Pump PLL)

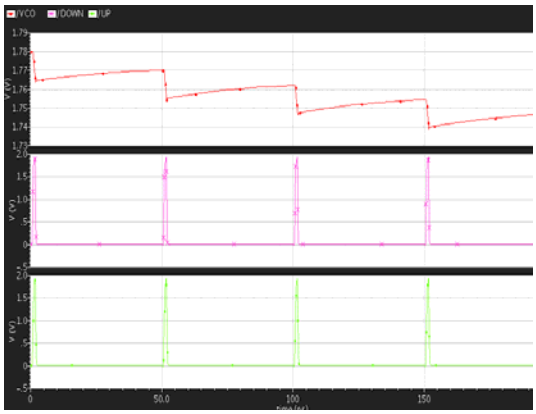

Figure 9: VCO control voltage when reference signal and feedback signal phase & frequencies are equal (Conventional Charge Pump PLL)

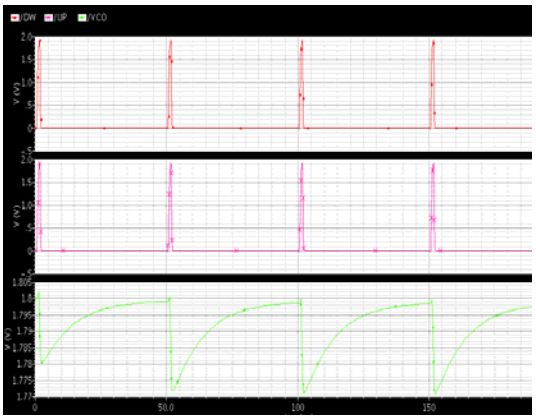

Figure 10: VCO control voltage when reference signal and feedback signal phase & frequencies are equal (Proposed Charge Pump PLL)

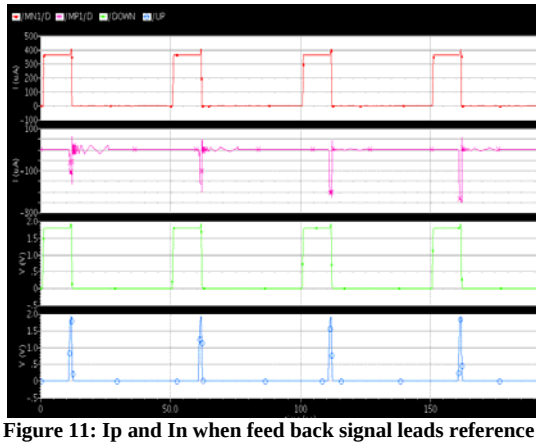

Figure 11: Ip and In when feed back signal leads reference signal in the proposed CP.

3.2 Equations

$$\Phi_{\varepsilon} = 2\pi \cdot \frac{\Delta t_{on}}{T_{ref}} \cdot \frac{\left| I_{UP} - I_{DN} \right|}{I_{cp}}$$

Equation (1)

$$\boldsymbol{Rout = R06.gm5.R05 \; at \; the \; node \; D}$$

Equation (2)

4. Conclusion

By using the gain-boosting and low-voltage cascode current mirrors, a high-performance low-mismatch charge pump is achieved. Good current matching characteristics can be achieved with less than 0.1% difference of the Up/Down current and 1% over all process variations. The CP output compliance voltage range of 0.1-1.8 V is achieved for 1.8-V supply voltage. Charge sharing problem can also be eliminated with the help of charge removal transistor and this proposed CP PLL also provides high gain by increasing the output impedance with the help of low voltage cascode current mirror. The circuit was designed using 0.18um TSMC CMOS technology and simulated by Spectre tools.

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