Temperature effects on the Drain Current in GaN Dual-Gate MESFET using Two-Dimensional Device Simulation

Hamida DJELTI[1], Mohammed FEHAM[1], Achour OUSLIMANI[2] and Abed-Elhak KASBARI[2]

**[1] Laboratoire des Systèmes et Technologies de l'Information et de la Communication (STIC)
Département de Génie Electrique, Faculté de Technologie
Université Abou Bekr Belkaid de Tlemcen
BP 230, Chetouane,13000 Tlemcen - Algérie**

**[2] ENSEA, Electronique et Commande de Systèmes ECS-Lab EA3649
6 avenue du Ponceau, 95014 Cergy Cedex, France**

Abstract

Temperature dependence of the GaN-Dual-Gate MESFET (GaN-DGMESFET) DC-characteristics is investigated using two dimensional numerical simulations. Differential equations derived from a Hydrodynamic electron transport model describe the physical proprieties of the device. Simulation results over a wide range of temperature from 300 K to 900 K performed on an industrial software Atlas from SILVACO are presented for a GaN-DGMESFET with a gate length of 0.5 µm. The results show a significant degradation of the DC characteristics. Variation of the electron temperature with the drain-source voltage (Vds) is studied and a large temperature is observed for Vds > 1 V. At low drain-source voltage (Vds < 1 V) the electron temperature is closed to the lattice temperature.

Keywords: *DGMESFET, GaN, Temperature, Steady-state.*

1. Introduction

In recent years, GaN-based field effect transistors (FETs) have emerged as a promising candidate for high power, high temperature microwave applications and power electronics. These devices' impressive performance is due to the material's properties, such as wide band gap, high breakdown field, and high electron saturation velocity [1, 2] and relatively high electron mobility. Because of the relatively higher band gap energy of GaN (3.47 eV at 300 K) the onset of diffusion-dominated leakage currents generally occurs at much higher temperatures than in GaAs. This provides a potential advantage for GaN IC's.

DGMESFET have been commonly used at very high frequency in many different applications such as gain controlled amplifiers, frequency multipliers, phase shifters, stabilised oscillators, power combiners and splitters, [3].

In general, a DGMESFET is basically modelled as a cascade connection of two single-gate MESFET's (SGMESFET) FET_1 and FET_2 as shown in figure 1, where each FET part has a current generator [4]. This configuration improves the output impedance, reduces the feedback capacitance and features a reduction of short-channel effects compared to those observed in single-gate FETs [5].

The temperature effect on the DC characteristics of GaAs DGMESFET for both planar and vertical structures over a wide range of temperature from 250 K to 400 K has been reported [6, 7, 8]. The temperature effects on the DC GaN-DGMESFET characteristics have received a little attention. Indeed, much of the working on the GaN MESFET devices has concentrated their effort on the DC, AC and noise [9, 10].

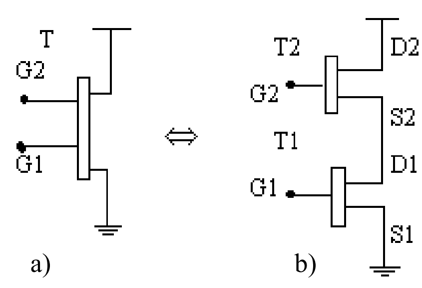

Fig. 1 Symbolic diagram of: (a) DGMESFET, (b) Cascade circuit of two SGMESFET's [4].

In this paper, we investigate the temperature dependence of the DC characteristics in 0.5 µm gate length GaN DGMESFET. The industrial software Atlas from SILVACO, is used to perform the two-dimensional numerical simulations. The transport properties of the GaN DGMESFET are described via differential equations derived from the Hydrodynamic electron transport model (HM). This model consists of an additional coupling of the current density to the carrier temperature.

In the following, section 2 describes the theoretical study of the temperature dependence of the DGMESFET drain current. The results and discussions of a 0.5 µm DGMESFET with a source-to-drain spacing of 3 µm are presented in section 3. Finally, the conclusion is presented in section 4.

2. Theoretical analysis of GaN DGMESFET

The most important main factors responsible for the change of DGMESFET performances with the temperature are: the energy band gap, the electron mobility, the saturation velocity and the threshold voltage. The band gap energy is modeled using [11]:

$$E_{gap}(T) = E_{gap}(T=300K) + \alpha\left[\frac{300^2}{300+\beta} - \frac{T_L^{\ 2}}{T_L+\beta}\right]$$
(1)

Where the values of α and β for GaN are respectively 0.909 10^{-3} eV/K and 774 K. T_L is the lattice temperature. Figure 2 shows the GaN band gap energy which decreases with increased temperature.

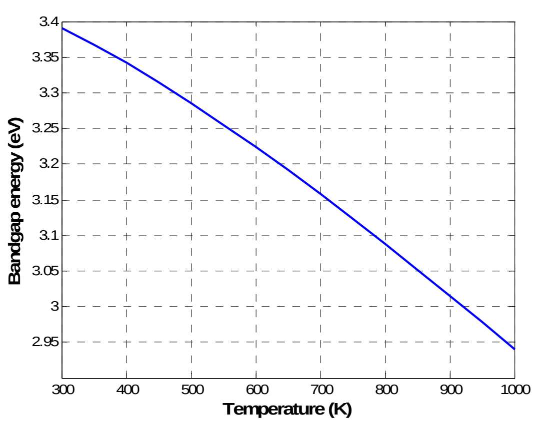

Fig. 2 Temperature dependence of energy band gap.

The empirical expression for the electron mobility suggested by Farahmand [12] is given by (2):

$$\mu_n(T,N) = \mu_{1n}\left(\frac{T_L}{300}\right)^{\beta} + \frac{(\mu_{2n} - \mu_{1n})\left(\frac{T_L}{300}\right)^{\Delta}}{1 + \left(\dfrac{N}{Ncrit\left(\frac{T_L}{300}\right)^{\gamma}}\right)^{\alpha\left(\frac{T_L}{300}\right)^{\varepsilon}}} \qquad (2)$$

Where the mobilities at low electric field μ_{1n} and μ_{2n} are respectively equal to 295 and 1460.7 cm^2/V.s, the quoted value of α, β, γ, Δ and ε are respectively equal to 0.66, -1.02, -3.84, 3.02, 0.81. *N* is the local impurity concentration and Ncrit is set to 10^{17} cm^{-3}.
Figure 3 shows the temperature effect on the electron mobility for three values of doping concentration (2x10^{17}, 2.5x10^{17} and 3x10^{17} cm^{-3}).
We note that the mobility decreases with increased temperature.

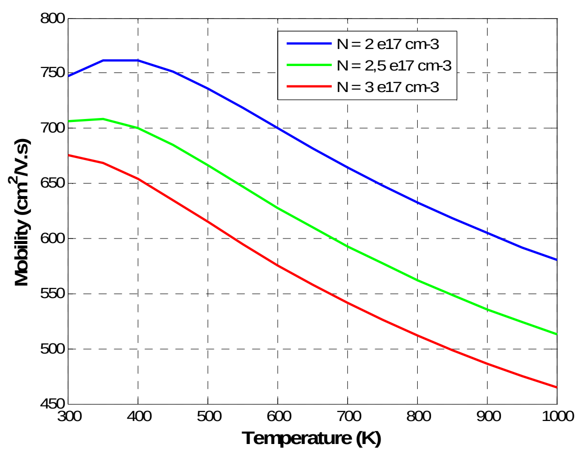

Fig. 3 Temperature effect on the electron mobility for three values doping concentrations.

The threshold voltage is the most significant parameter in study of the temperature dependence of DGMESFET characteristics. The temperature variation of threshold voltage is given by:

$$V_{th} = V_{bi} - V_p \qquad (3)$$

Where V_p is the pinch-off voltage and V_{bi} is the Schottky barrier height given by [13]:

$$V_{bi}(T) = V_{bi}(T0) + m[E_{Gap}(T) - E_{Gap}(T0)] \qquad (4)$$

In (4), m is between 0 and 1.
Figure 4 shows the temperature variations of threshold voltage. The threshold voltage decreases approximately linearly with increased temperature.

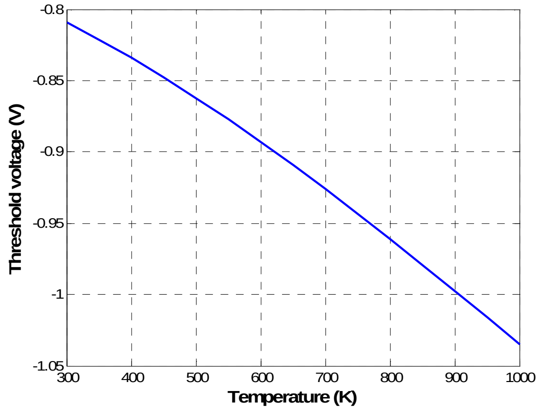

Fig. 4 Temperature dependence of the threshold voltage .

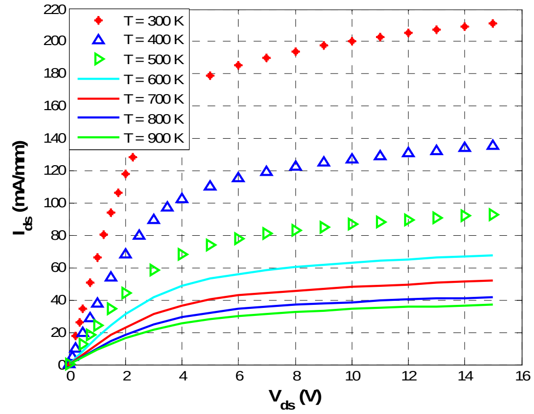

Fig. 6 DGMESFET output characteristics at Vgs1 = 0.0 V and Vgs2 = -0.25 V for different temperatures.

3. Simulated results and discussions

Figure 5 shows the studied DGMESFET structure. Figure 6 depicts the DGMESFET output Ids-Vds characteristics for different temperatures from T = 300 to 900 K, with a step of 100 K. The gates biases are Vgs1 = 0.0 V and Vgs2 = - 0.25 V.
The conduction along the channel in DGMESFET is influenced by the temperature dependence of certain parameters. As shown in figure 6, the drain current decreases with increased temperature, indeed, if the temperature increases the thermal agitation of carrier's increases, this leads to decrease the mobility of carriers in the cannel, and in particular to greatly affect their velocity.

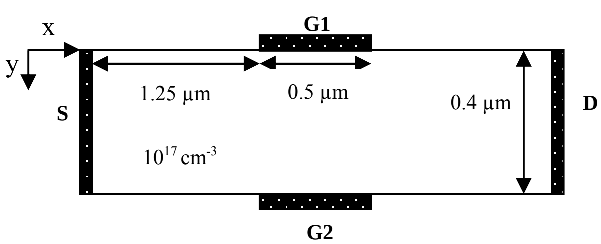

Fig. 5 Cross-section structure of the simulated DGMESFET.

The transfer characteristics of the DGMESFET at different temperatures (T = 300 to 900 K, with a step of 100 K), for a gate2-source voltage of 0.0 V and for a drain-source voltage of 5 V are shown in figure 7. We have used the drain bias of 5 V because for this polarization the transistor operates in the saturation region. Figure 7 gives an Idsmax of a 224 mA/mm at room temperature. The threshold voltage defined as the intercept point of the gate voltage and the linear extrapolation of the Ids versus Vgs characteristics at the maximum transconductance point, is of a - 8 V at room temperature.

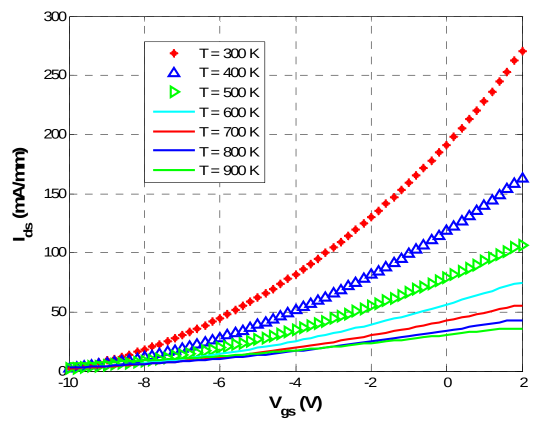

Fig. 7 DGMESFET Ids-Vgs characteristics at Vds = 5 V.

In order to investigate the electron temperature in the channel of the DGMESFET, figure 8 shows the variations of the electron temperature with the applied drain bias as a function of the gates bias at a point (x = 2.8 µm; y = 0.2 µm located near the drain contact. As shown in figure 8, we can see that, the electron temperature is close to the lattice temperature at low drain voltages. Due to the existence of a high electric field in the gate-to-drain region, a large electron temperature is observed when the drain voltage is greater than 1 V.

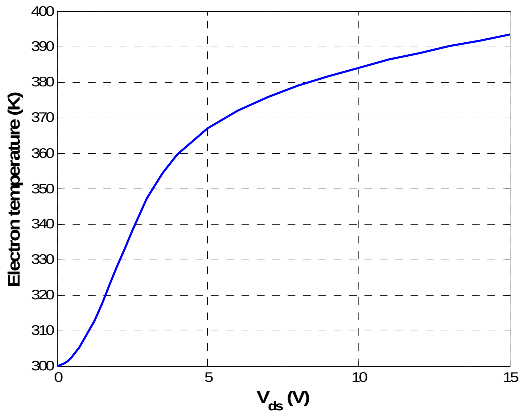

Fig. 8 Electron temperature versus drain voltage near the drain contact (x = 2.8 µm; y = 0.2 µm), Vgs1 = Vgs2 = 0 V.

4. Conclusions

In this paper, a study of the DC characteristics temperature dependence of a 0.5 µm GaN Dual-Gate MESFET is presented. Significant physical proprieties of the device have been described using differential equations derived from a Hydrodynamic electron transport model. Two dimensional numerical simulations results over a wide range of temperatures have been presented and discussed. Degradations of the DC characteristics of the device have been observed at higher temperatures. A large electron temperature is also observed for a drain to source voltage greater than 1 V. For a low drain-source voltage (Vds < 1 V) the electron temperature is closed to the lattice temperature.

References

[1] C. Lee, W. L u, E. Piner, I. Adesida, "DC and microwave performance of recessed-gate GaN MESFETs using ICP-RIE", Solid-State Electronics, Vol. 46, 2002, pp. 743–746.

[2] Valentin O. Turina and Alexander A. Balandin, "Electrothermal simulation of the self-heating effects in GaN-based field-effect transistors", Journal of Applied Pysics, Vol. 100, 2006, pp. 054501.

[3] M. Schoon, "A novel, bias-dependent, small-signal model of the dual-gate MESFET", *IEEE Trans.* Microwave Theory Tech., Vol. 42, 1994, pp.212-216.

[4] M. Ibrahim, B. Syrett, and J. Bennett, "A new analytical small-signal model of dual-gate GaAs MESFET", IEEE MTT-S International Microwave Symposium Digest, 2001, pp. 1277-1280.

[5] M. W. Dvorak "InAs/AlSb Heterostructure Field-Effect Transistors", Master Thesis, Simon Fraser University August, 1997.

[6] H. Djelti, M. Feham, M. Kameche, A. Ouslimani, "On the advantages of GaAs dual-gate MESFET's in comparison to Single-gate MESFET's", 2nd International Conference on Information & Communication Technologies from Theory to Applications - ICTTA'06, 2006, Vol. 2, pp. 2562-2566.

[7] H. Djelti, M. Feham, M. Kameche, A.Ouslimani "Temperature Effect on the Drain Current of Dual-Gate GaAs MESFET's", HITEN'2005, France.

[8] M. Kameche, "Drain temperature determination in dual-gate GaAs MESFETs", Journal of computational electronics, Vol. 6, 2007, pp. 421-424.

[9] N. Lakhdar and F. Djeffal**,** "A two-dimensional analytical model of subthreshold behavior to study the scaling capability of deep submicron double-gate GaN-MESFETs", Journal of Computational Electronics, Vol. 10, No. 4, 2011, pp. 382-387.

[10]: N. Lakhdar, F. Djeffal, M.A. Abdi, D. Arar, "An analytical threshold voltage model to study the scaling capability of deep submicron double-gate GaN-MESFETs", XIth International Workshop on Symbolic and Numerical Methods, Modeling and Applications to Circuit Design, 2010, pp. 1-4.

[11] S.-M. Sze, "Physics of Semiconductor Devices", New York: John Wiley, 1981.

[12] Farahmand, M. et. al., "Monte Carlo Simulation of Electron Transport in the III-Nitride Wurtzite Phase Materials System: Binaries and Terniaries", *IEEE* Trans. Electron Devices, Vol. 48, No. 3, 2001, pp. 535-542.

[13] M. Kameche, and N.V. Drozdovski, "GaAs-, InP- and GaN HEMT-based Microwave Control Devices: What is Best and Why", Microwave J., Vol. 48, No. 5, 2005, pp. 164-180.