DSP Implementation of a Power Factor Correction Strategy for BLDC Motor Drive

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Abstract

The paper develops a power factor correction mechanism for a brushless dc permanent magnet (BLDC-PM) motor drive system through the use of a front end boost converter. It evolves a wave shaping mechanism to arrive at the sinusoidal nature for the input current in an effort to improve the input power factor. The theory is articulated using a closed loop algorithm to revolve around the operating range of the drive motor. The performance is evaluated on a MATLAB platform to elucidate the viability of the scheme in addition to highlighting its speed regulating capability. It steals the role of a Digital Signal Processor (DSP) to implement the proposed methodology and there from validate the results with a view to illustrate its practical applicability.

1. Introduction

Power Factor Correction (PFC) circuits appear to occupy the input stages in almost every medium and high power switching power supply systems operating at the voltage mains. The most often used configuration includes a boost converter at the primary stage, stabilizing the input to the second stage. Conventional off-line power converters with front - end diode-capacitor rectifier inherit a distorted input current waveform with high harmonic content. Though a variety of passive and active PFC techniques are in vogue, the passive techniques may be the best choice only in low-power and cost sensitive applications. Besides the dc voltage on the energy-storage capacitor in a single-stage PFC converter is not regulated.

The Brushless DC motors (BLDC) continues to attract the drive industry owing to its simplicity, low-cost and robust structure and it is suitable for variable-speed applications. The structure though simple draws a pulsating AC line current resulting in low power factor and high harmonic line current. However with the increasing demand for improved power quality, there is a definite need for better strategies to accomplish a high performance BLDC motor drive.

A novel power factor correction strategy suitable for brushless DC motors has been suggested [1]. It has been found to eliminate the use of boost unity power factor stage and bulk electrolytic capacitors. An algorithm for power factor correction of direct torque controlled brushless DC motor drive in the constant torque region has been outlined [2]. An intelligent power factor correction methodology based artificial neural network has been proposed [3]. The dynamic characteristics of the brushless DC motor and the currents & voltages of inverter components have been analyzed through the use of fuzzy logic controller [4]. The current controlled mechanism has been found to allow the re-generative braking of BLDC motor and resultant improving the efficiency and lowering the acoustic noise [5]. It augurs the use of a power-factor-correction mechanism appropriately interfaced with a BLDC motor driver circuit to arrive at the desired quality of power.

1.1. Problem Definition

The primary focus is to design a control algorithm that envisage to improve the input power factor of an inverter fed BLDC motor drive in addition to regulating its speed. It attempts to incorporate an AC - DC boost converter at the front end and builds a comprehensive closed loop strategy to reshape the nature of the input current wave. The addition of boost interface adds to the advantages of high efficiency and power density.

2. Proposed Strategy

A boost converter is controlled by pre - calculated duty cycles to land at sinusoidal input current waveform. The input voltage feed - forward compensation enables the output voltage to be insensitive to the input voltage variation and guarantees the sinusoidal input current even if the input voltage is distorted. The methodology is evaluated through simulation and validated using a Digital Signal Processor (DSP) based prototype over the entire operating range.

The power module of the proposed approach is displayed in Fig.1 shows the boost converter cascaded with an inverter to power the BLDC motor. The Hall sensors

imbibed in the rotor provide the necessary feedback to regulate the speed.

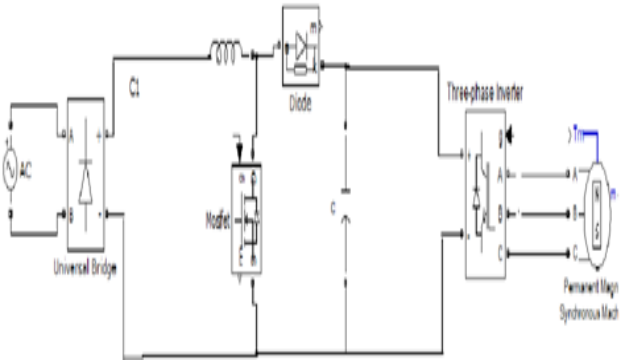

Fig .1 Power Module

3. Control Algorithm

The objective of the control scheme of the boost converter is to regulate the power flow ensuring the tight output voltage regulation as well as unity input power factor. The modeling equations of various components of the converter system are formulated separately to develop a comprehensive model for their performance evaluation. The supply system under normal operating conditions can be modeled as a sinusoidal voltage source of amplitude Vm and frequency fs. The instantaneous voltage is given as:

$$V_s(t) = V_m \sin wt \quad (1)$$

Where

$$w = 2\pi f_s t$$

And t is the instantaneous time.

A template u(t) is estimated for converter topologies with AC side inductor, from the sensed voltage

$$u(t) = v_s(t) / V_m \quad (2)$$

u (t) for converter topologies with dc side inductor is obtained from:

$$u(t) = |V_s(t)| / V_m \quad (3)$$

The converters are modeled using first order non-linear differential equations. The number of equations is equal to the number of energy storage components in the system. The Single-phase boost PFC converter is modeled using two differential equations for inductor current i_L and DC link capacitor voltage V_{DC} .

$$pi_L = (\upsilon_d - \upsilon_p) / L - r(i_L / L) \quad (4)$$

$$p\upsilon_{dc} = (i_p - \upsilon_{dc} / R) / C_d \quad (5)$$

Where p is the differential operator (d/dt), r is the internal resistance of the inductor L, V_d is the rectified line voltage of diode rectifier output, R is the resistance of the load and V_p is the PWM voltage across the switch and is defined as

$$V_p = V_{DC}(1 - s) \quad (6)$$

i_p is the current through the boost diode and is defined as

$$i_p = i_L(1 - S) \quad (7)$$

Where S is the switching signal obtained from current regulation loop. Its value is 1 (ON) or 0 (OFF) depending upon the state of the switch.

The Fig.2 shows the Schematic diagram of AC-DC boost type PF controller where the output of voltage regulator is limited to a safe value and forms the amplitude of input reference current. This reference amplitude is then multiplied to a template of input voltage to synchronize the reference with input voltage, as required for unity power factor operation. The inductor current is forced to track its reference current using current controller, which generates the appropriate gating signals for the active device.

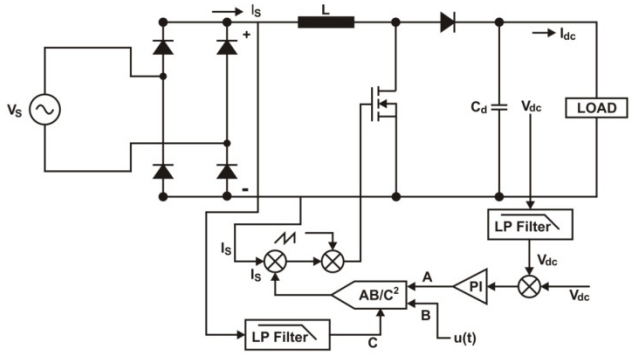

Fig. 2 Schematic diagram of AC-DC boost type PF controller

A proportional integral (PI) voltage controller is selected for voltage loop for tight regulation of the output voltage. The DC voltage V_{DC} is sensed and compared with set reference voltage V_{DC}*.

The resulting voltage error $v_{e(n)}$ at nth sampling instant is:

$$\upsilon_{e(n)} = \upsilon^*_{dc} - \upsilon_{dc(n)} \quad (8)$$

Output of PI voltage regulator $v_{o(n)}$ at *n*th sampling instant is:

$$\upsilon_{\theta(n)} = \upsilon_{\theta(n-1)} + K_p(\upsilon_{e(n)} - \upsilon_{e(n-1)}) + K_i \upsilon_{e(n)} \quad (9)$$

Where K_P and K_i are the proportional and integral gain constants. Ve (n.1) is the error at the $(n.1)^{th}$ sampling instant. The output of the controller $V_{0(n)}$ after limiting to a safe permissible value is taken as amplitude of reference supply current. The current regulation loop is required for active wave shaping of input current to achieve unity input power factor and reduced harmonics. The input voltage template B is obtained from the sensed supply voltage and is multiplied with the amplitude of reference source current A in the multiplier-divider circuit. Moreover, a component of input voltage feed forward C is also added to improve the dynamic response of the converter system to line disturbances. The resulting signal forms the reference for input current. The instantaneous value of the reference current is given as:

$$i_s^* = AB/C^2 \quad (10)$$

The inductor current error is the difference between the reference supply current and inductor current (i_{en}=is*-is). This error signal is amplified and compared to the fixed frequency carrier wave to generate the gating signals for power switches.

4. Simulation

The scheme is simulated using MATLAB to investigate the performance of 310V, 4.2 A 3400 rpm and 1.1 HP BLDC motor. The Fig .3 depicts the input voltage and the input current at an operating point corresponding to 0.5 Kw, brought in phase due to the action of the PFC. The Comparisons of the input power factors over the entire range of load powers are elucidated through Fig. 4 to highlight the significant role of the PFC.

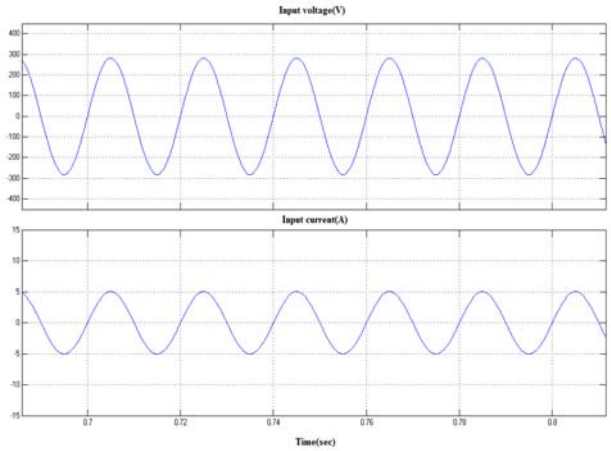

Fig .3 Input Voltage and current of PFC

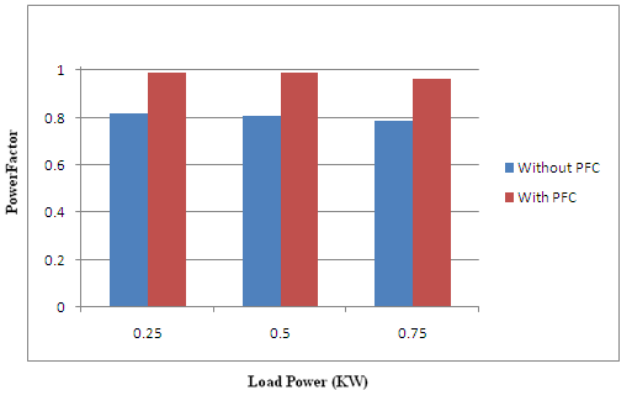

Fig .4 Comparison of Power Factor with and without PFC

5. Hardware Implementation

The Performance of the algorithm is experimentally tested on the BLDC motor of similar ratings with DSP TMS320FC2812 based control to identify the numerous non-topological factors that affect the quality of current drawn by the converter. The power circuit is fabricated with IRFP460 MOSFET and MUR460 fast recovery diode with Ls = 1.1 mH and Cd = 560mF. The converter is fed from AC lines through an autotransformer followed by an isolation transformer to provide variable input voltage and protection, respectively.

The DSPs are designed for closed loop control implementations are extensively used in areas of motor control, UPS, and motion control applications.
The Fig.5 shows a power factor corrector (PFC) stage interfaced to a TMS320LF2407A DSP. It is the AC-DC boost converter stage that converts the AC input voltage to a high voltage DC bus and maintains sinusoidal input current at high input power factor. As indicated in Fig.5, three signals (the rectified input voltage Vin, the inductor current Iin, and the DC bus capacitor voltage Vo) are required to implement the control algorithm and the converter is controlled by two feedback loops. The average output DC voltage is regulated by a slow response 'outer loop' whereas, the inner loop shapes the input current is a much faster loop.

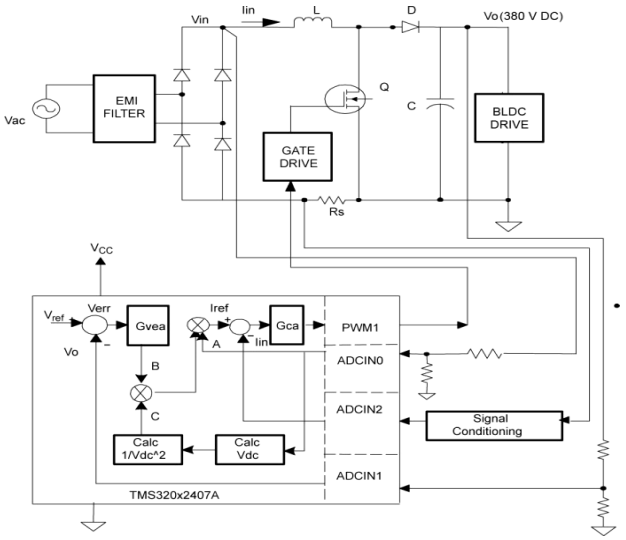

Fig .5 TMS320LF2812 Controlled Power Factor Corrector (PFC) Stage for BLDC Drive

The instantaneous signals Vin, Vo and Iin are all sensed and conditioned by the respective voltage and current sense circuits. The sensed signals are then fed back to the DSP via three ADC channels ADCIN0, ADCIN1, and ADCIN2 respectively. The rate at which these signals are sensed and converted by the ADC is called the control loop sampling frequency fs. The digitalized sensed bus voltage Vo is compared to the desired reference bus voltage Vref. The difference signal (Vref - Vo) is then fed into the voltage loop controller Gvea. The digitized output of the controller Gvea, indicated as 'B', is multiplied by two other components, 'A' and 'C', to generate the reference current command for the inner current loop. The component 'C' is calculated as,

$$C = \frac{1}{V_{DC} \times V_{DC}}$$

Where Vdc is the calculated average component of the sensed digitized signal Vin. In Fig.5, Iref is the reference current command for the inner current loop. Iref takes the shape of a rectified sine wave and its amplitude maintains the DC output voltage with a reference level Vref against the variation in load and fluctuation in line voltage. The sensed digitized inductor current Iin is compared with the reference current Iref. The difference between Iref and Iin is passed into the current controller Gca. The output of this controller is finally used to generate the PWM duty ratio command for the PFC switch.

The Fig.5 (a) shows the control loop block diagram of the DSP controlled PFC converter. In this figure, the voltage and current sense/conditioning circuits are replaced by their respective gain blocks.

These blocks are indicated as K_f, K_s and K_d. The multiplier gain K_m is also added to the control block and it allows the adjustments of the reference signal I_{ref} based on the converter input operating voltage.

The inner loop is the current loop which is programmed by the reference current signal I_{ref}. The input to the current loop power stage is the duty ratio command d and its output is the inductor current I_{in}. The current controller G_{ca} is designed to generate the appropriate control output U_{ca} such that the inductor current I_{in} follows the reference current Iref. The outer voltage loop is programmed by the reference voltage command V_{ref}. The input to the voltage loop power stage is U_{nv} (voltage controller output) and its output is the dc bus voltage Vo. The voltage controller G_{vea} is designed to generate the appropriate U_{nv} to control the amplitude of the reference current I_{ref} such that for the applied load current and line voltage, the bus voltage Vo is maintained at the reference level.

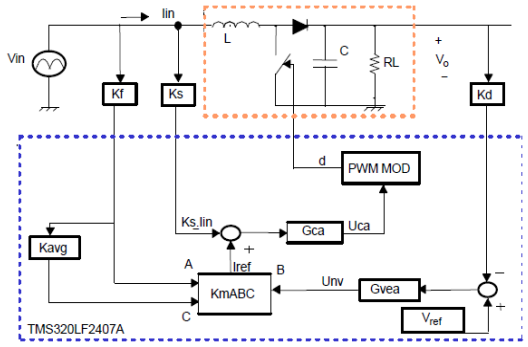

Fig. 5(a) Control Loop Block Diagram of the DSP Controlled PFC Stage

Fig. 6 Flow chart for DSP program

6. Experimental Results

The performance of the experimental prototype is investigated over the same operating range and the results obtained are displayed through Figs. 7 to 9. The PWM pulses to the power switches in the inverter at the chosen operating point are displayed in Fig. 7. The speed – time relationship established in Fig. 9 explains its regulatory action owing to the influence of the closed loop algorithm even when the BLDC motor is subjected to a sudden ten percent change both in reference speed and load. The input voltage and current waveforms in Fig.8 serves to validate the simulated response.

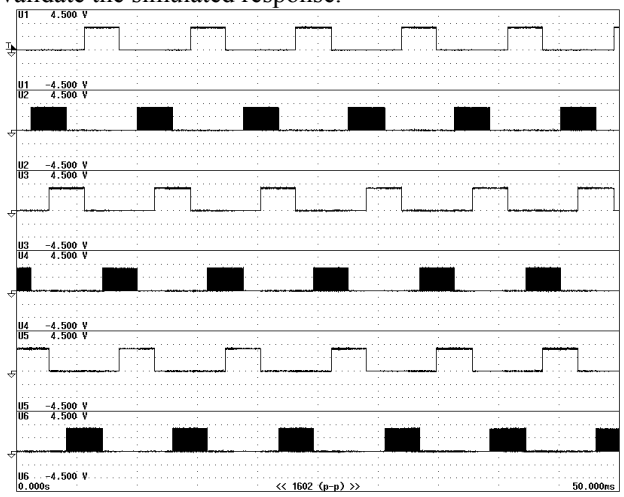

Fig .7 PWM pulses for inverter

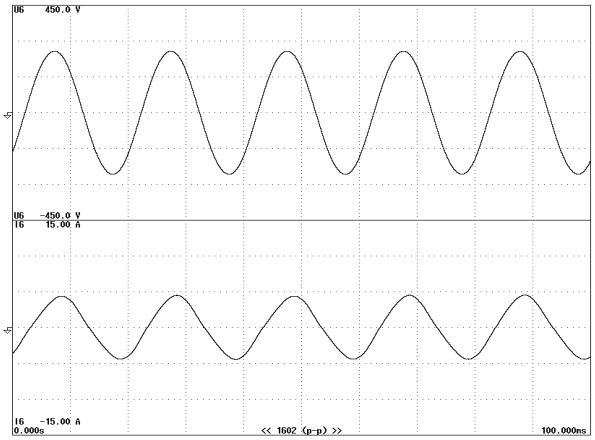

Fig .8 Source voltage and current wave

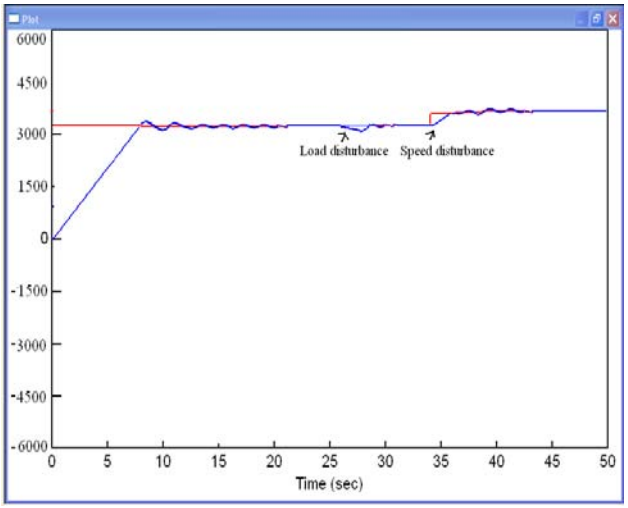

Fig .9 speed regulation graph

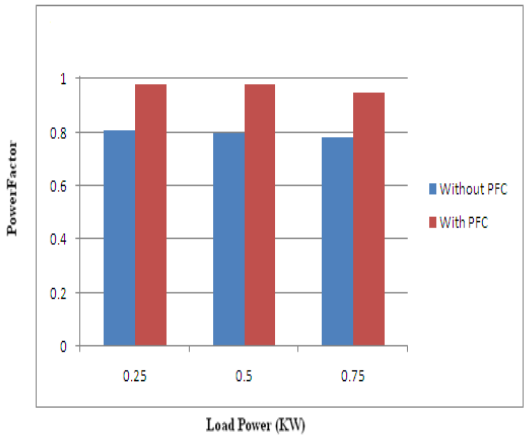

Fig .10 Comparison of Power Factor with and without PFC

The bar diagram displayed in the Fig.10 highlights the significant improvement in input powerfactor, adequately validated through DSP based prototype. With the load power allowed to vary across an appropriate operating range the experimental readings are compared with simulated results in Table.1 to validate the proposed methodology and highlight its suitability for practical applications.

S.no	Load power(KW)	Input current(A)	Input voltage(V)	Output current(A)	Speed(RPM)		Powerfactor	
					simulation	DSP	simulation	DSP
1	0.25	2.3	240	1.05	3400	3400	0.991	0.982
2	0.5	3.1	239	2.6	3400	3400	0.989	0.981
3	0.75	4.14	230	3.1	3400	3400	0.965	0.95

Table .1 Performance comparison in simulation and real time implementation

Conclusion

An average current control algorithm has been developed for the BLDC drive to achieve input power factor through the use of a boost topology. The scheme has been formulated using high switching frequency PWM signals generated based on current feedback. The distortion in the input current has been corrected by triggering the power factor controller and shaping the input current wave into the desired sinusoid. A prototype has been constructed using a DSP controller board and ML4821 IC and the performance evaluated.

The experimental results have been found to adequately validate the simulated response and exhibit the suitability of the use of DSPs in this domain. The exercise has been found to illustrate the suitability of the proposed algorithm for practical systems and will go a long way in nurturing further innovative applications for BLDC motors.

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