Low-Power and High Speed 128-Point Pipline FFT/IFFT Processor for OFDM Applications

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ABSTRACT

This paper represents low power and high speed 128-point pipelined Fast Fourier Transform (FFT) and its inverse Fast Fourier Transform (IFFT) processor for OFDM. The Modified architecture also provides concept of ROM module and variable length support from 128~2048 point for FFT/IFFT for OFDM applications such as digital audio broadcasting (DAB), digital video broadcasting-terrestrial (DVB-T), asymmetric digital subscriber loop (ADSL) and very-high-speed digital subscriber loop (VDSL). The 128-point architecture consists of an optimized pipeline implementation based on Radix-2 butterfly processor Element. To reduce power consumption and chip area, special current-mode SRAMs are adopted to replace shift registers in the delay lines. In low-power operation, when the supply voltage is scaled down to 2.3 V, the processor consumes 176mW when it runs at 17.8 MHz.

KEYWORDS

Low power, FFT, IFFT, OFDM

INTRODUCTION

The FFT (Fast Fourier Transform) and its inverse (IFFT) are the key components of OFDM (Orthogonal Frequency Division Multiplexing) systems. Recently, the demand for long length, high-speed and low-power FFT has increased in the OFDM applications. There are three kinds of main design architectures for implementing a FFT processor. One is the single-memory architecture. It has one processing element and one main memory. Hence, it occupies a small area. The second is the dual-memory architecture, which has two memories. This architecture has a higher throughput than the single-memory architecture because it can store butterfly outputs and read butterfly inputs at the same time. The fast Fourier transform plays an important role in many digital signal processing (DSP) systems. Recent advances in semiconductor processing technology have enabled the deployment of dedicated FFT processors in applications such as telecommunications, speech and image processing. Specifically, in the OFDM communication systems, FFT and inverse FFT (IFFT) play a very important role. The OFDM technique, due to its effectiveness in overcoming adverse channel effects [1, 2] as well as spectrum utilization, has become widely adopted in wire line and wireless communication standards.

The OFDM technique has been adopted in several standards like digital audio broadcasting (DAB) [3], digital video broadcasting-terrestrial (DVB-T) [4], asymmetrical digital subscriber line (ADSL) [5] and very-high-speed digital subscriber line (VDSL) [6]. Therefore, efficient and low-power VLSI implementation of FFT processors is essential for successful deployment of these OFDM-based systems. According to the standards of DAB, DVB-T, ADSL and VDSL, various FFT sizes are required, as shown in Table 1. From this Table, it is clear that variable-length FFT hardware is a crucial module in the low-cost solution of the above communication systems.

The Cooley – Tukey N-point FFT algorithm requires O(Nlog N) computations, which is a huge saving over direct computation of the discrete Fourier transform (DFT). However, hardware implementation of the algorithm is both computational intensive, in terms of arithmetic operations, and communication intensive, in terms of data swapping. For real-time processing of FFT, O(log N) arithmetic operations are required per sample cycle. High speed real-time processing can be accomplished in two different ways. In the conventional general-purpose digital signal processor (DSP) approach, the computation is carried out by a single processor driven to a high clock frequency, which is O(log N) times the data sample frequency. In the application-specific parallel or pipelined processor approach, the required operations are performed at the clock frequency equivalent to the sample frequency, and this approach usually consumes less power.

In this paper, we aim to implement a low-power variable-length FFT processor. To this end, we adopt several optimization techniques in the circuit design to accomplish an area- and power-efficient pipelined FFT processor.

Pipelined FFT/IFFT processor Architecture

Radix-2 FFT/IFFT architecture

The radix-2 multi-path delay commutator [7] is a pipelined implementation of the radix-2 FFT/IFFT algorithm. A radix-2 multi-path delay commutator architecture with N ¼ 8 is shown in Fig. 1. The input sequence is divided into two parallel data streams by a commutator and then, with proper scheduling for two streams, butterfly operation in a processing element (PE)

and twiddle factor multiplication is executed. In total, ($\log_2 N$ -2) multipliers, log2 N radix-2 butterfly units, and (3N/2) -2 delay elements are

Communication system	OFDM Size
ADSL	512
VDSL	8192,4096,2048,1024,512
DAB	2048,1024,512,256
DVB-T	8192,2048

Required. With a proper input buffering scheme, the processing element can work at 100% utilization.Radix-2 single-path delay feedback architecture (shown in Fig. 2) utilizes the delay elements more efficiently by sharing the same storage between the butterfly outputs and inputs [8]. A single data stream goes through the multiplier at every stage. This architecture has the same number of processing elements (PEs) and multipliers as needed in the radix-2 multi-path delay commutator architecture, albeit only N 1 delay elements. Note that the butterfly units and multipliers work at 50% utilization since half of the time they are bypassed.

2.2 Radix-2=4=8 FFT/IFFT algorithm and architecture

The N-point DFT is formulated as

$$x_z = \sum_{n=0}^{N-1} xnW^{nz}, z = 0,1,2,.....N-1$$

Where $W^{nz} = e^{-j2\pi\frac{nz}{N}}$ The basic concept underlying the radix-2 FFT/IFFT algorithm is the use of symmetry between the twiddle factors W^{nz} and $W^{nz+N/2}$ ($W^{nz} = -W^{nz+N/2}$).

Exploiting twiddle factor symmetry further, the multiplication by the twiddle factors of $W^{N/8}$, $W^{3N/8}$, $W^{5N/8}$ and $W^{7N/8}$ can be further simplified since their real and imaginary parts have equal magnitude. The complex multiplications by these four twiddle factors can be formulated as:

$$(a + jb)W^{N/8} = -(a + jb)W^{5N/8}$$

$$= \frac{\sqrt{2}}{2}[(a+b) + j(b-a)]$$

$$(a + jb)W^{3N/8} = -(a + jb)W^{7N/8}$$

$$= \frac{\sqrt{2}}{2}[(b - a) - j(a + b)]$$

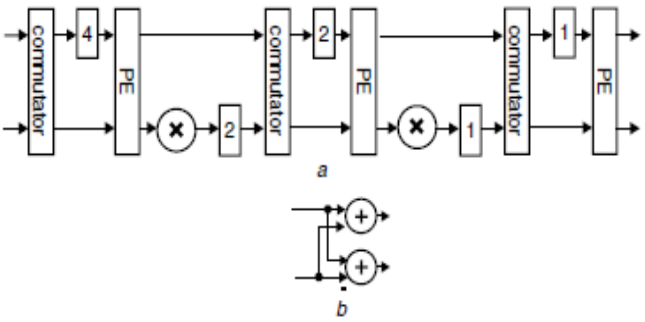

Fig. 1 Radix-2 multi-path delay commutator FFT/IFFT architecture and PE

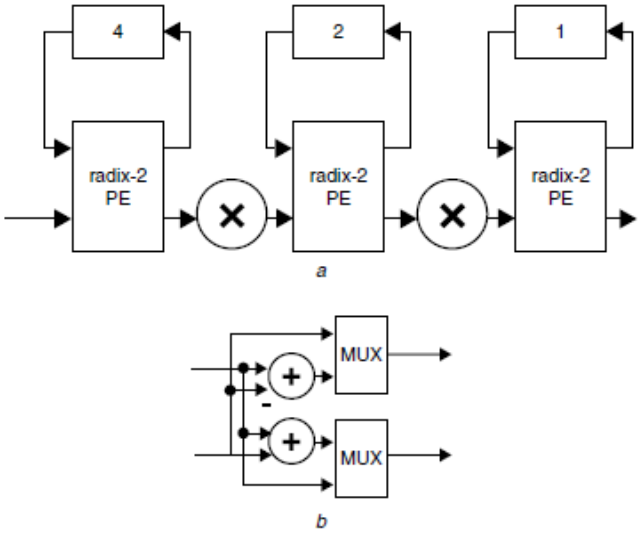

Fig. 2 Radix-2 single-path delay feedback FFT architecture, and PE

Note that these complex multiplications can be realized by two real multiplications and two additions.

The signal flow graph (SFG) of the radix-2=4=8 FFT/IFFT algorithm is shown in Fig. 3 [9]. Instead of one single butterfly, the radix-2=4=8 algorithm implements the radix-8 butterfly using three radix-2 stages. Therefore its SFG is equivalent to that of the radix-2^3 algorithm [10]. Note that by modifying the radix-2 single-path delay feedback FFT/IFFT architecture, a radix-2=4=8 architecture was proposed in [9]. There are three types of basic processing elements, called PE1, PE2 and PE3, and each processes one FFT stage. The architecture is made up of a repeated cascade of PE1, PE2, PE3 and a general complex multiplier for twiddle-factor multiplication. The number of delay elements needed decreases by half in every stage. The block diagrams of these three types of processing elements are illustrated in Fig. 4.

2.3 Proposed variable-length FFT/IFFT processor architecture

At the architecture level, to reduce power consumption and chip area, it is desirable to adopt the FFT algorithm which has least computational complexity and the architecture that corresponds to less hardware complexity. The block diagram of the proposed variable-length FFT processor based on the radix-2=4=8 single-path delay feedback architecture is depicted in Fig. 5. The proposed processor can perform FFT operations of three

different lengths: 2048-point, 1024-point and 128-point. To accommodate different numbers of FFT stages, the first two stages are radix-2 PEs, which have the same structure as the PE3 unit in the radix-2=4=8 architecture, and each of the following three blocks is made up of a set of PE1, PE2 and PE3 and a twiddle-factor multiplier. If 512-point FFT is executed, then input signals skip the first two stages through the control of the multiplexer, MUX2. If a 128-point FFT is performed, the first stage is bypassed through MUX1.

3 Architecture considerations

3.1 Comparison of FFT architectures

Over the years, various FFT architectures have been proposed with a view to providing speedy and efficient implementation of the all-important FFT operation. In Table 2, we list some computational features the radix-2=4=8 FFT architecture used in the proposed IC and

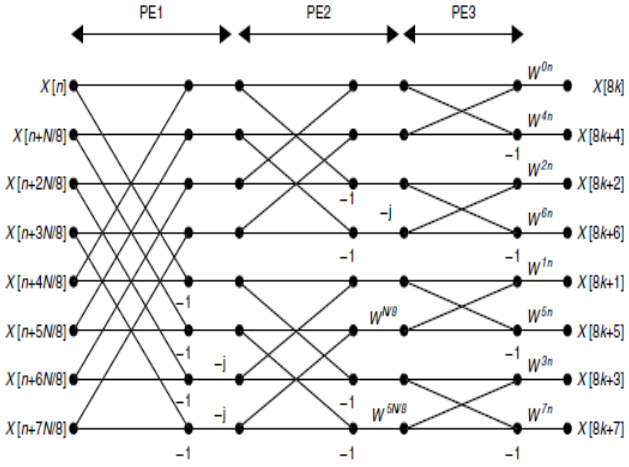

Fig. 3 Signal flow graph of the radix-2=4=8 FFT/IFFT algorithm

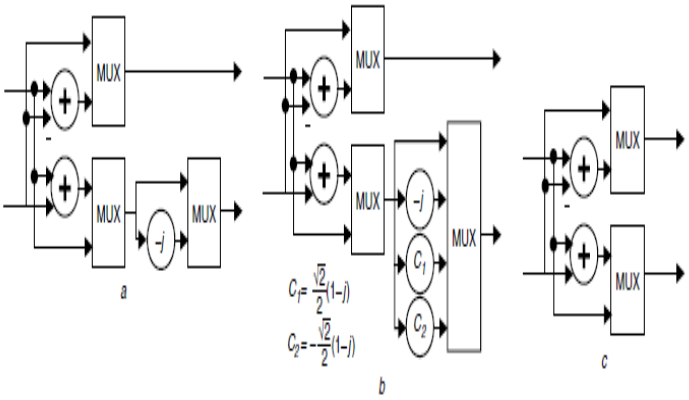

Fig. 4 Block diagrams of the PE units in the radix-2=4=8 architecturePE1 PE2 PE3

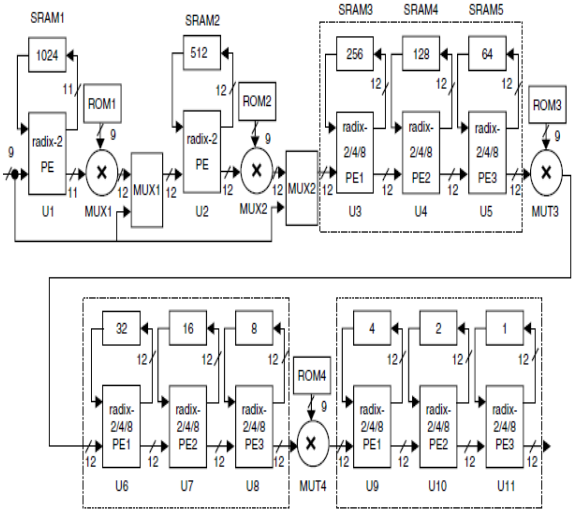

Fig. 5 Block diagram of proposed variable-length FFT/IFFT processor

Several other recent architectures. In the Table, we compare their computational complexity and memory requirements. It is apparent that the number of nontrivial complex multiplications decreases as the radix gets higher.

In addition, in bit-parallel operation, higher-radix algorithms also have better hardware utilization in multipliers. As to the adders in butterfly units, if the higher radix butterfly operation is implemented by concatenating radix-2

Table 2: Comparison of several FFT architectures

	Bit-parallel			Digit-serial
	Proposed chip	He & Torkelson [10]	Hui et al. [Chang & Parhi [12]	
Radix	radix-2=4=8	radix-4	radix-4	radix-4
Data flow	feedback	feedback	Feed forward	Feed forward
Complex adder utilization	$2 \log_2 N$	$4 \log_4 N$	$12 \log_4 N$	$8(\log_4 N + 1)$
Complex multiplier utilization	50%	50%	100%	100%
Data memory	$\log_8 N$ 7 1	$\log_4 N$ 7 1	$3(\log_4 N$- 7 1)	$3(\log_4 N$ -7 - 1)
Twiddle factor ROM	87:5%	75%	100%	100%
	N 7 1	N 7 1	2.5N	1.18N
	0.25N	N	N	0.5N

butterfly units, such as in [10], then only 50% adder utilization can be achieved. Note that in the digit-serial architectures [11, 12], the word-length of the data in adders and multipliers is reduced to one digit and thus fewer full adders are required. On the other hand, to achieve almost 100% utilization in adders and multipliers, the word-length of the signals in these two architectures must be restricted to match the throughputs of the radix-4 commutator – 4 digits in these cases. Nevertheless, the occupied area of one complex multiplier overwhelms the area of one complex adder. Thus, a great saving in the cost of silicon can be accomplished with fewer complex multipliers.

Feedback FFT architecture needs the least amount of data memory, in the size of N 1. On the other hand, feed-forward architecture requires more memory elements, as in [11, 12]. Other memory blocks are the look-up-table ROMs that store twiddle factors. If the number of nontrivial complex multiplications is decreased, then there are fewer twiddle-factor ROMs. The twiddle-factor ROM for the first multiplier stores twiddle factors with a phase spacing of 2p=N. In the later stages, the phase spacing increases. If the symmetry of the sine=cosine function is further exploited, more saving in ROM size can be had. In the proposed chip, the twiddle-factor ROMs store only one-eighth cycle of the sine=cosine waveforms and we take advantage of the symmetry of all the twiddle factors instead of the redundancy within each group of W^n, W^{2n} and W^{3n}, for n ¼ 0; 1; . . . ; N=4, in the radix-4 algorithm as in [12], and consequently a smaller ROM table is built.

In summary, the radix-2=4=8 algorithm can bring forth a variable-length FFT processor with the least overall hardware complexity. Although its adder and multiplier utilization is not as good as other architectures, we decide to adopt this architecture because it strikes a balance between hardware complexity and computational efficiency.

3.2 Complex multiplier against CORDIC

The CORDIC algorithm has been used for the twiddle factor multiplication in FFT processors due to its efficiency in vector rotation [13]. In this sub-Section, we evaluate and compare the performance and complexity of a CORDIC and a complex multiplier in phase rotation. In Table 3, the conventional CORDIC algorithm refers to the radix-2 CORDIC, and radix-2=4 CORDIC refers to the work in [14] that enhances operation speed and reduces 25% of the micro-rotation stages. The complex multiplier used in the proposed chip consists of three multiplications and five additions [15]. To make a fair comparison, we set the precision to 16 bits in all algorithms. To avoid rounding error propagation [14, 16], 19 bits are allocated in the data path of the CORDIC-based architectures.

In the conventional CORDIC algorithm, a ROM table that stores the rotation sequences with N=4 16-bit words in the range of ½0; p=2& is used. Two 19-bit adders are required in each micro-rotation stage and the conventional CORDIC architecture needs 2 16 19 ¼ 608 full adders for 16 micro-rotation stages. Additional constant multiplication by 0.100110110111010 as the scaling factor is performed in the final scaling stage and it needs 2 9 19 adders. Without pipelining, its critical path delay is 19 16 times the full adder delay (T_{FA}) in the 16 micro-rotation stages plus 28 T_{FA} in the scaling stage.

In [14], the ROM table is further reduced to N=8 words with 23 bits per word due to the higher radix adopted in the later stages. According to the authors, each stage is based on a similar cell with a 4-2 adder=subtracted using two-level carry– save adders (CSA) and redundant arithmetic representation intended to improve the performance. Two registers are used to buffer the intermediate sum and carry in each stage. Meanwhile two full adders are connected to perform the 4-2 compression. As a result, a total of 2 19 17 2 full adders are provided in the 17 stages including additional micro-rotation-repetition stages and 2 scaling stages. Because of pipelining in every stage, the critical path delay is reduced to about $2T_{FA}$ with a penalty of a large number of ð17 19 2 2Þ pipeline registers. Actually, its CORDIC outputs are still in the form of redundant arithmetic representation and will be transformed back to the binary format after butterfly operation by carry-look ahead adders.

In the proposed chip, complex multiplication consists of five real additions and three real multiplications. The real addition is implemented by carry-selected adders with a maximum delay of about $8T_{FA}$ and each utilizes 30 full adders in the first 16-bit addition and 63 full adders in the last 33-bit addition. Because Wallace tree multipliers are adopted for the three 16 17 multiplications, the critical path delay is reduced to $7T_{FA}$. One 16 17 Wallace tree multiplier needs about 280 full adders, and two pipeline stages are inserted before and after the multiplication.

We can see that the CORDIC algorithm may be too slow without pipelining. On the other hand, Wallace tree multiplication reduces the critical path delay of the complex multiplier approach. Considering all aspects of speed –area tradeoff and that the application of the FFT processor is low power consumption rather than high speed, we use the complex multiplier for twiddle factor multiplication.

4 Circuit design

To serve as a key component in OFDM communication systems, the variable-length FFT processor must be designed to reduce its power consumption as well as chip

4.1 Word-length minimization

In the design of this application-specific variable-length FFT processor, the word lengths of various signals are minimized according to their respective signal-to-noise ratio (SNR) requirements. To decide the optimal word length, input waveforms with Gaussian noise are fed to the FFT with fixed-point arithmetic implementation. The frequency-domain FFT output signals are obtained and the output signal-to-noise ratio (SNR) is computed. Figure 6a shows the output SNR against the FFT input word length under different input SNR conditions. Accordingly, the word length of the input is set to 9 bits. As to the precision of the sine and cosine tables, the output SNR against the word length of the twiddle factors is shown in Fig. 6b when the input signal has an SNR of 30 dB. A word length of 9 bits is thus chosen for the twiddle factors. The word-length minimization process then goes on module by module and the word lengths of all signals in the processor are determined, and are labeled in Fig. 5. Conventional address decoder since data to and from the SRAM is accessed sequentially. To further conserve power consumption, true-single-phase-clock (TSPC) flip-flops are used in the ring counters.

4.3 Current-mode SRAM

The current-mode technique has been used in reading SRAM cell contents. It has been proposed that the current-mode technique can also be applied to the writing operation of SRAM so as to further reduce power consumption [18]. This is because voltage swings of the SRAM bit lines and data lines can be kept very small in the current-mode read=write operations and thus the dynamic power dissipation can be significantly decreased.

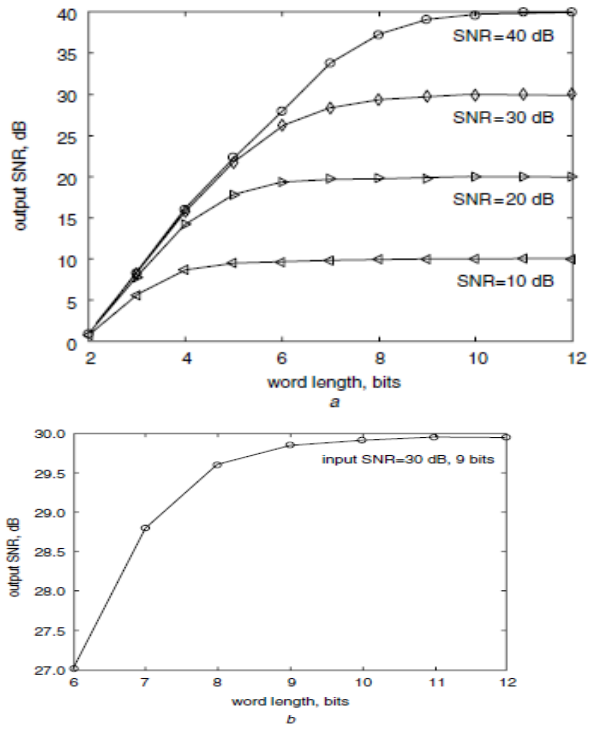

Fig. 6 Output SNR against word length of the FFT processor input and of twiddle factor

4.2 RAM-based delay line

A single-path delay feedback FFT processor needs several long and wide delay lines. Conventionally, delay lines are mostly implemented in shift registers, made up of cascades of data registers, as shown in Fig. 7a. At each clock edge, all data move forward in a lock-step fashion and approximately half of the registers change states, wasting much power. To save power and chip area, SRAM has been utilised to replace the shift registers. Since the read and write operations must be performed in one clock cycle, intuitively a dual-port memory is required. Two single-port SRAMs are adopted in [17], and the authors claimed that a single-port memory can save 33% in area over a dual-port memory. Here we use one single-port SRAM as shown in Fig. 7b. The SRAM is designed manually. In the first half clock cycle, the read operation is performed while the write operation follows in the next half clock cycle. To prevent the data access of the SRAM becoming critical paths, two registers, one before the PE and the other after, are inserted. Furthermore, a ring counter is used instead of the

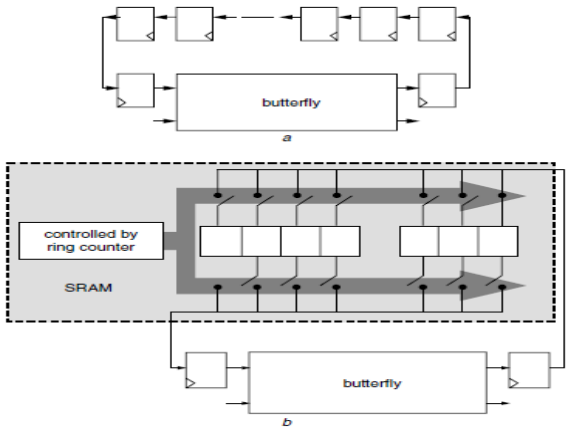

Fig. 7 Conventional shift-register-based delay line and proposed SRAM-based delay line

The current-mode SRAM cell used is based on that proposed in [18], and it consists of seven transistors, one more than the conventional 6-transistor SRAM cell, and it is depicted in Fig. 8a. An extra transistor, M_{eq}, is inserted to equalize the output voltages of the two inverters before each write operation, and therefore a small current difference can be sensed through access transistors controlled by the

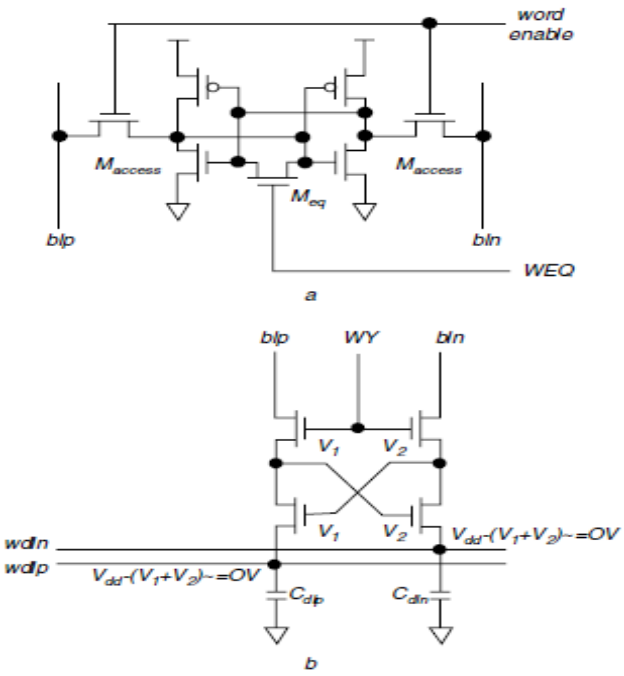

Fig. 8 Schematic diagrams of proposed 7T current-mode SRAM memory cell and of SRAM write circuitry using N-type current conveyor

Word-line enable signal and amplified by the inverters. When M_{eq} is off, the cell performs as the conventional 6T SRAM memory cell.

During write access, a current difference, *D*I, appears on the write data lines wdlp and wdln. The N-type current conveyor (shown in Fig. 8b) is enabled by the signal WY. Then the currents are conveyed to the bit lines blp and bln without attenuation. Because the control signal WY is enabled, a virtual short circuit exists between the write data lines wdlp and wdln. Both the voltages at wdlp and wdln are equal to V_{DD} ðV$_1$ þ V$_2$Þ, which can be designed to approach the ground voltage. Thus the voltage swing on data lines can be kept as small as possible. The read operation in this SRAM is implemented by a sense amplifier, which has the same structure as the conventional SRAM, and a column decoder. As in conventional SRAM, a read access starts with the word line being enabled and the pair of bit lines driven by a differential current, which is then steered to the sense amplifier, where the data are sensed and buffered.

4.4 Complex multiplication and twiddle-factor ROM

In the proposed FFT processor, due to the radix-2=4=8 algorithm, each complex multiplication of $W^{N=8}$, $W^{3N=8}$, $W^{5N=8}$ and $W_p^{7N=8}$ is reduced to two real multiplications by the constant 2=2 as shown in (2) and (3), which can be further simplified to shift and add operations [9].

5 Experimental results

The whole chip, except for the SRAM modules, was designed by a gate-level hardware description language. The critical path lies in the complex multiplier. The layout of the SRAM modules containing the ring counters, timing control units as well as the SRAM cells are all designed manually. This proposed FFT processor is fabricated using a 0:35 *m*m CMOS process. The chip's die photo is shown in Fig. 10. The multipliers are marked as MUT with their corresponding twiddle-factor ROMs right beside, and the PEs for processing elements are labeled as Ux. Considering circuit overheads in SRAM, all delay lines longer than 64 are implemented by SRAM, while shorter ones are realized by registers. A brief summary of the chip is given in Table 3.There was an error made in some of the ROM values but, discounting that error, the rest of the chip can operate as designed. The FFT processor can operate up to 17.8 MHz and dissipates 176mW at 2.3V supply voltage and it can operate up to 45 MHz at 3.3V supply voltage when it consumes 640 mW
Comparisons of the proposed chip with several FFT processors [9, 17, 20, 21], including FFT size, algorithm, process, supply voltage, power consumption, clock rate, execution time and area. Because these FFT processors are fabricated in different CMOS technologies and the FFT sizes are also different, it is not easy to make a fair comparison. We adopted three indices to make comparisons and adjusted the numbers by estimation assuming all processors perform a 1024-point FFT. We use the normalized area, a metric in [21], and it is given by

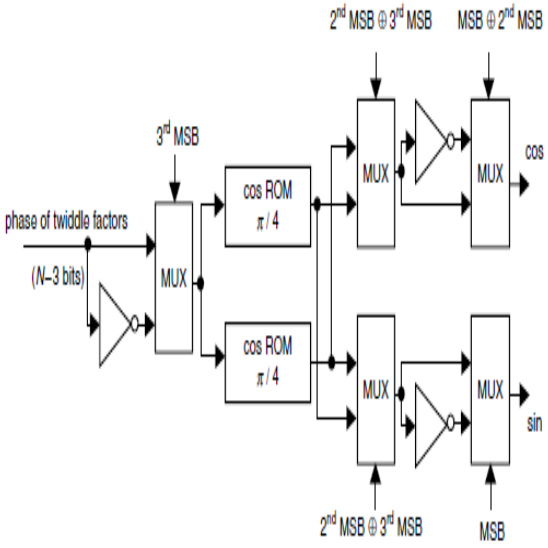

Fig. 9 Block diagram of twiddle-factor ROM

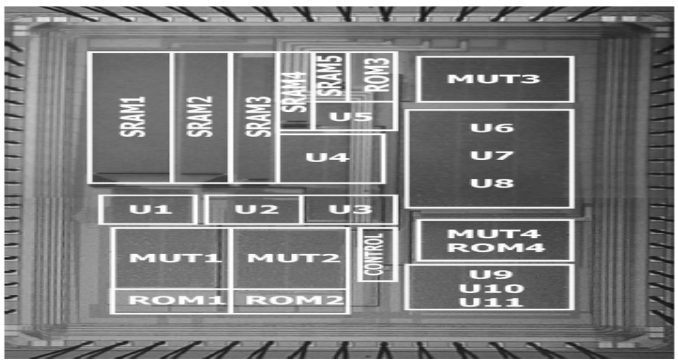

Fig. 10 Die photograph of proposed FFT processor

Normalized area =Area of 1024 - point FFT/Technology/(0:35μm)^2.
FFT/Energy =Technology/Power of 1024 - point FFT * Execution Time *10^{-6}

Another metric considering both energy efficiency and speed performance is the energy–time product, and it is given by

Energy * Time =Execution Time/FFT/Energy

We can see from the Table that the proposed chip has the smallest normalized area and the smallest energy–time product. Although the FFT processor in [21] has the best energy efficiency when operating at 1.1 V, its slow execution speed at that low voltage prevents it from high-speed applications in Table 1.

Table 3 chip summary

Process	TSMC 0.35 1P4M
Area	3:9mm_ 5:5mm
Transistor count	598 078
Maximum frequency	45MHz at 3.3V
Power consumption (at highest speed)	640mW (at 45 MHz, 3.3 V)
Power consumption (at lowest voltage)	176mW (at 17.8 MHz, 2.3 V)
Package	68 PGA

6 Conclusions

In this paper, we have reported the design of an FFT/IFFT processor chip that is suitable for OFDM communication systems, such as DAB, DVB-T, ADSL and VDSL, for performing complex FFTs/IFFT of lengths 128=1024=2048. The proposed variable-length FFT processor not only achieves efficient hardware utilization but also low power consumption. It's a dual-path delay feedback FFT/IFFT architecture requires fewer delay elements and the radix-2=4=8 FFT algorithm replaces some complex multipliers with shift and-add operations. In addition, some other circuit techniques have been applied for saving complexity as well as power consumption. The chip was implemented using a 0:35 *m*m CMOS process. The measured results show that the chip can operate up to 45MHz under a 3.3-V supply voltage and it consumes 640 mW. When the supply voltage is scaled down to 2.3 V, this processor consumes only 176mW when it runs at 17.8 MHz

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