Implementation of the OFDM Physical Layer Using FPGA

M.A. Mohamed[1], A.S. Samarah[1], M.I. Fath Allah[2]

[1] Faculty of Engineering-Mansoura University-Egypt

[2] Delta Academy of Science for Engineering and Technology-Egypt

ABSTRACT

Orthogonal Frequency Division Multiplexing (OFDM) transmissions are emerging as important modulation technique because of its capacity of ensuring high level robustness against interference. OFDM is a modulation technique which is now widely used in various high speed mobile and wireless communication systems as; fixed Wi-Fi system (IEEE 802.11a standard), mobile Wi-Fi system (IEEE 802.11b standard), fixed WiMAX system (IEEE 802.16a standard), and mobile WiMAX system (IEEE 802.16e standard). In this paper the design and implementation of OFDM system will be illustrated as well as a detailed simulation of the OFDM system using MATLAB-2011 program to study the effect of various design parameters on the system performance, also the design and simulation results for some standards of OFDM using MATLAB will be observed as a practical system examples that uses OFDM as a modulation technique. OFDM transceiver will be implemented using FPGA Spartan 3A kit. All modules are designed using VHDL programming language.

Keywords: *Orthogonal Frequency Division Multiplexing (OFDM); Field Programmable Gate Array (FPGA); Hardware Description Language (HDL); Inverse Fast Fourier Transform (IFFT); Fast Fourier Transform (FFT); Cyclic Prefix (CP); Bit Error Rate (BER); Signal to Noise Ratio (SNR).*

1. INTRODUCTION

OFDM could be tracked to 1950's but it had become very popular at these days, allowing high speeds at wireless communications [1]. While OFDM has become the core of most 4G communication systems as fixed Wi-Fi system (IEEE802.11a standard), mobile Wi-Fi system (IEEE802.11b standard), fixed WiMAX system (IEEE802.16a standard), mobile WiMAX system (IEEE802.16e standard), and Long Term Evolution (LTE) system; it was essential to build this OFDM system on a suitable hard ware.

The aim of our paper is to implement this system to be suitable for all new communication systems. FPGAs are flexible and reconfigurable integrated circuits, whose functionality is programmed by the designer rather than the device manufacturer. Unlike an Application- Specific Integrated Circuit (ASIC), FPGAs can be reprogrammed multiple times, even after deployment. The high speed, parallel architecture provides complete control over the degree of parallelism in the design, and arithmetic word lengths. This flexibility is a key advantage of FPGAs over traditional Digital Signal Processor (DSP) processors. Many recent high speed digital signal processing applications such as networking, video and image processing and communications are implemented by using FPGA [2]. In our implementation, the emulation time has been made as short as possible.

The resources of Xilinx Spartan-3A kit have been suitable for our implementation. This paper aims to give an idea of what is an OFDM system, its implementation and the analysis of the obtained results of the simulations testing. This OFDM system is able to support different M-QAM modulation schemes. The next of this paper is organized as follows; section-2 provides the related work, section-3 introduces OFDM overview, section-4 presents simulation results, section-5 introduces VHDL emulation and conclusions.

2. RELATED WORK

Moisés Serra [3] shows the design of an OFDM transmitter as a part of an OFDM demonstrator Hiperlan/2 based, Ma. José Canet [4] shows implementation issues of a digital transmitter for an OFDM based WLAN systems and benchmarks some optimized VHDL area results against System Generator results, Canet's work is focused on the solutions for the OFDM signal generation in base-band and in intermediate frequency (IF). Chris Dick [5] emphasizes the suitability of high-level design tools when designing sophisticated systems, and the importance to design FPGA systems rather than ASIC to one day accomplish the SDR "Software Defined Radio" concept and gives a high-level overview of the FPGA implementation giving some deep to the synchronization, packet detection, preamble correlate channel estimation and equalization; that is mainly at the OFDM receiver.

Ludovico de Souza et al. [6] present a FPGA implementation capable to support 802.11 wireless modems but just as a validating and prototyping stage for an ASIC. Joaquin Garcia, Rene Cumplido [7] focuses on the FPGA suitability to support IF processing for the Std. IEEE 802.11a and the resource area and timing

requirements either for rapid prototyping or to take advantage of re-configurability in order to be able to support different standards. Y. Awad, L. H. Crockett and R. W. Stewart [8] investigate the efficient FPGA implementation of an OFDM transceiver design for the IEEE 802.20 physical layer. Paul Guanming Lin [9] demonstrates the concept and feasibility of an OFDM system, and investigates how its performance is changed by varying some of its major parameters. This objective is met by developing a MATLAB program to simulate a basic OFDM system. M. A. Mohamed [10] presents an FPGA technique to gain approach in the problem of OFDM system implementation.

3. OFDM OVERVIEW

OFDM is an attractive modulation scheme used in broadband wireless systems that encounter large delay spreads. OFDM avoids temporal equalization altogether, using a cyclic prefix technique with a small penalty in channel capacity. Where Line-of-Sight (LoS) cannot be achieved, there is likely to be significant multipath dispersion, which could limit the maximum data rate. Technologies like OFDM are probably best placed to overcome these, allowing nearly arbitrary data rates on dispersive channels. [11]. Each subcarrier can be modulated independently as shown in Fig. 1. The spectra of the subcarriers overlap, but the subcarrier signals are mutually orthogonal as shown in Fig. 2 [11].

3.1 OFDM Advantages

In general, OFDM systems have the following advantages: (i) efficient use of spectrum.; (ii) resistant to frequency selective fading; (iii) Eliminates ISI (Inter-Symbol Interference) and ICI (Inter-Carrier Interference); (iv) can recover lost symbols due to the frequency selectivity of channels; (v) channel equalization; (vi) computationally efficient [11].

3.2 OFDM Disadvantages

OFDM systems have the following disadvantages: (i) High synchronism accuracy; (ii) Multipath propagation must be avoided in other orthogonality not be affected, and (iii) Large peak-to-mean power ratio due to the superposition of all subcarrier signals, this can become a distortion problem (Crest Factor) [11].

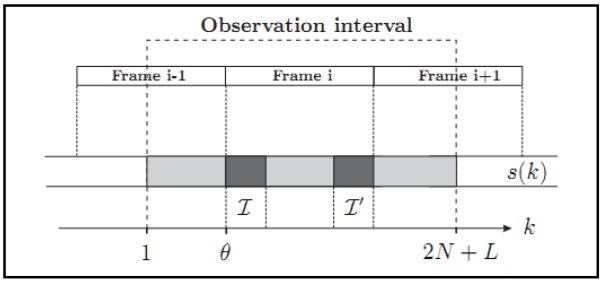


Fig.1 Structure of OFDM signal with cyclic extended frames

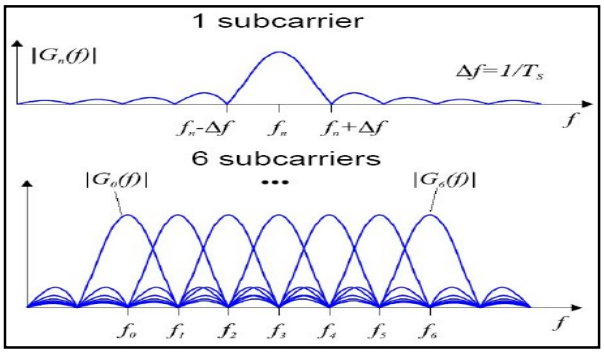


Fig. 2 OFDM Subcarriers in Frequency Domain

3.3 OFDM Transceiver

The block diagram of an OFDM transceiver is shown in Fig. 3. [9]. The basic component will be discussed in the next few subsections.

3.3.1 OFDM Transmitter

The main components of OFDM transmitter are shown in Fig.3 [9]. The randomizer is used as random bit generator. The first three blocks are used for data coding and interleaving. The coded bits will be mapped by the constellation modulator using Gray codification, this way an + jbn values are obtained in the constellation of the modulator. The serial to parallel converter converts the data bits from the serial form to the parallel form. The Inverse Fast Fourier Transform (IFFT) transforms the signals from the frequency domain to the time domain; an IFFT converts a number of complex data points, of length that is power of 2, into the same number of points but in the time domain. The number of subcarriers determines how many sub-bands the available spectrum is split into [11, 12]. The Cyclic Prefix (CP) is a copy of the last N samples from the IFFT, which are placed at the beginning of the OFDM frame to overcome ISI problem. It is important to choose the minimum necessary CP to maximize the efficiency of the system [16].

3.3.2 OFDM Receiver

The main blocks of OFDM receiver are observed in Fig.3 [9]. The received signal goes through the cyclic prefix removal and a serial-to-parallel converter [11]. After that, the signals are passed through an N-point fast Fourier transform to convert the signal to frequency domain. The output of the FFT is formed from the first M samples of the output. The demodulation can be made by DFT, or better, by FFT, that is it efficient implementation that can be used reducing the time of processing and the used hardware [14]. FFT calculates DFT with a great reduction in the amount of operations, leaving several existent redundancies in the direct calculation of DFT [13-15].

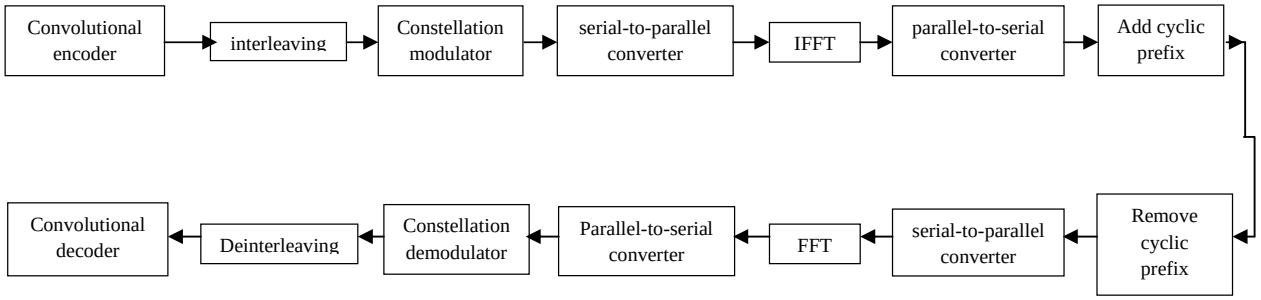


Fig. 3 OFDM Transceiver

4. Simulation Results

The presented OFDM system in the above few subsections will be simulated using MATLAB-2011 on a personal computer of the following specifications: (i) Intel processor 3.2 GHZ Pentium-four; (ii) 2MB cache RAM; (iii) 2 GB RAM; (iv) SATA hard disk 250GB. In this part the simulation of OFDM system using MATLAB Simulink tools will be obtained. The effect of different parameters on the simulation of the OFDM system using MATLAB program is discussed through the following experiments.

4.1 Experiment-1

In this experiment, the study of changing FFT/IFFT length with fixed SNR will be discussed. The optimum practical value used for the SNR is 60 dB in the case of using Additive White Gaussian Noise (AWGN) channel. The FFT/IFFT lengths that have been used are 8-points, 16-points, 32-points, 64-points, 128-points, 256-points, 512 points, and 1024 points. This experiment has been applied on OFDM system with 16-QAM. The simulation results for this experiment are shown in the following figures.

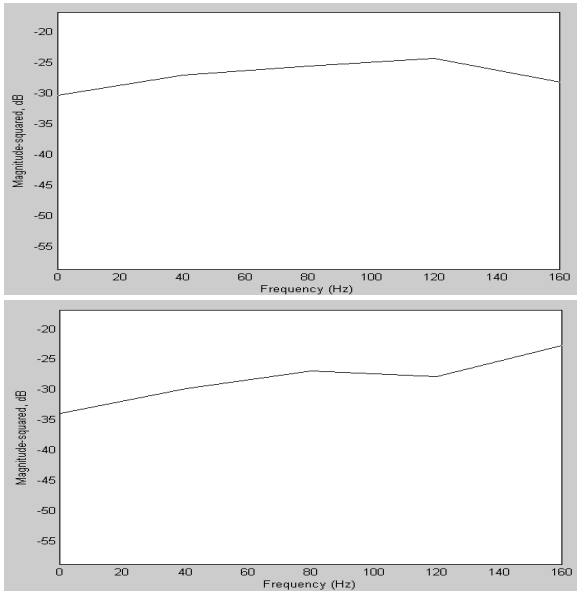


Fig. 4 OFDM with 16-QAM, 8-points IFFT/FFT with SNR=60 dB

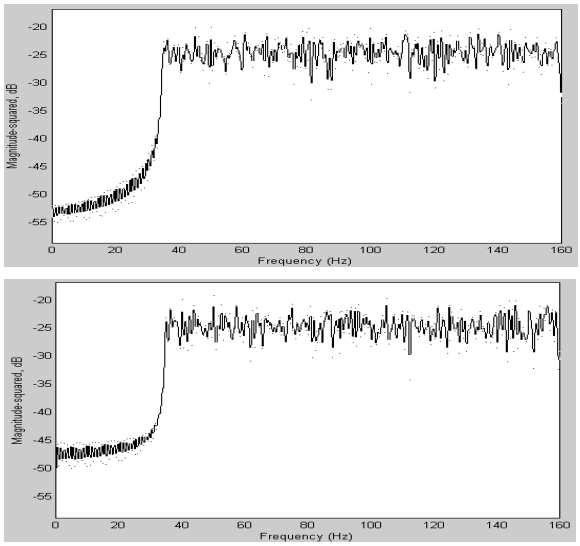


Fig. 5 OFDM with 16-QAM, 1024-points IFFT/FFT with SNR=60 dB

The simulation results for the worst case (8-points FFT) and the best case (1024-points FFT) were presented in the above figures for OFDM with 16-QAM. The result from this experiment is that the more FFT/IFFT length, the more accurate and more practical use of OFDM system; i.e. more subcarriers can be used as shown from the spectra of OFDM signals that are observed in the previouse figures.

4.2 Experiment-2

In this experiment the study of changing the SNR with fixed FFT/IFFT length will be discussed. The optimum length used for FFT/IFFT is 1024-points as discussed in experiment-1. The SNR values will be from 10dB to 60dB by step of 1dB. This experiment has been applied on OFDM system with 16-QAM. The simulation results for this experiment are shown in the following figures.

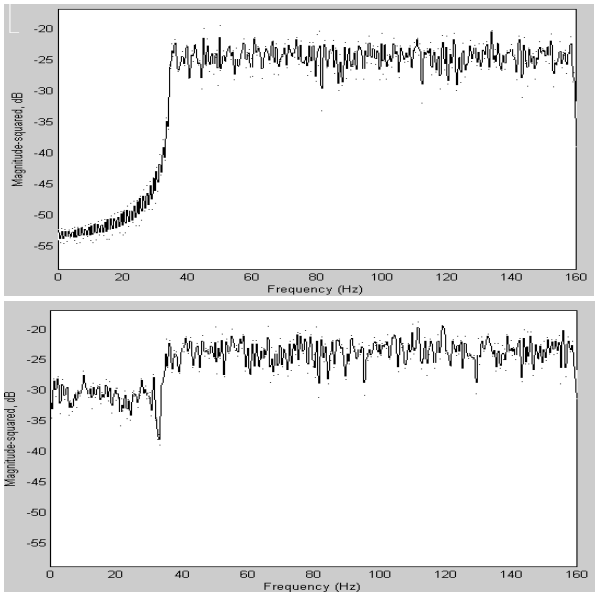


Fig. 6 OFDM with 16-QAM, 1024-points IFFT/FFT with SNR=10 dB

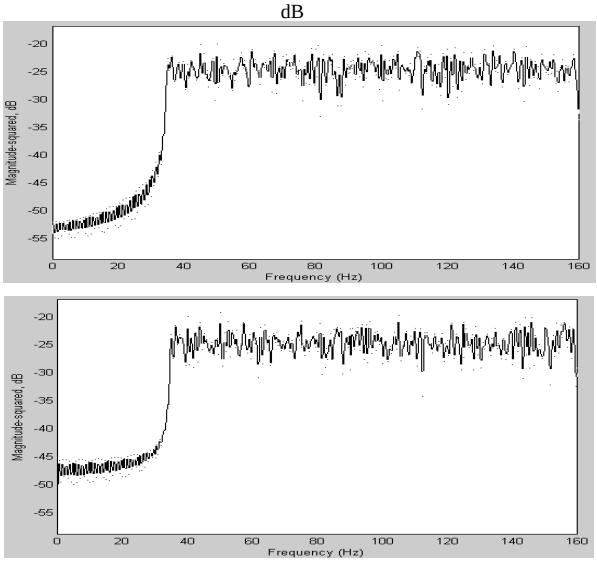


Fig. 7 OFDM with 16-QAM, 1024-points IFFT/FFT with SNR=60 dB

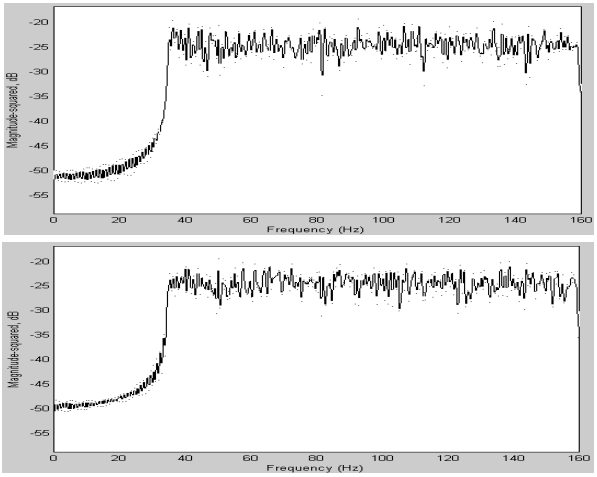


Fig. 8 OFDM with 16-QAM, 1024-points IFFT/FFT with SNR=70 dB

figures for OFDM with 4-QAM, 16-QAM, 64-QAM. From the results of this experiment, we get that the optimum value for the SNR is 60dB for minimum AWGN. After this value there is nearly no effect.

4.3 Experiment-3

In this experiment we discuss the effect of changing of the SNR over the scatter plot for complex digital modulator/demodulator with the same SNR values as in experiment-2. This experiment has been applied on OFDM system with 16-QAM. The simulation results for this experiment are shown in the following figures.

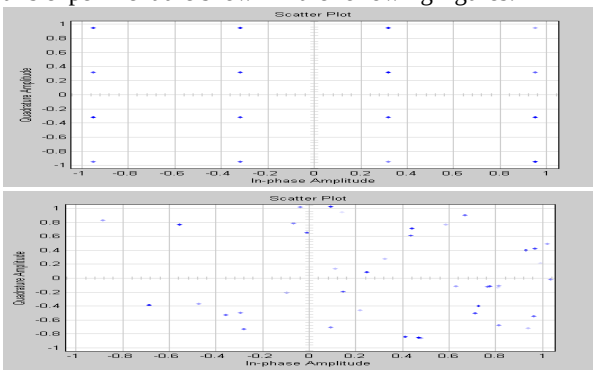


Fig. 9 OFDM with 16-QAM; scatter plot for modulator/demodulator, SNR=10 dB

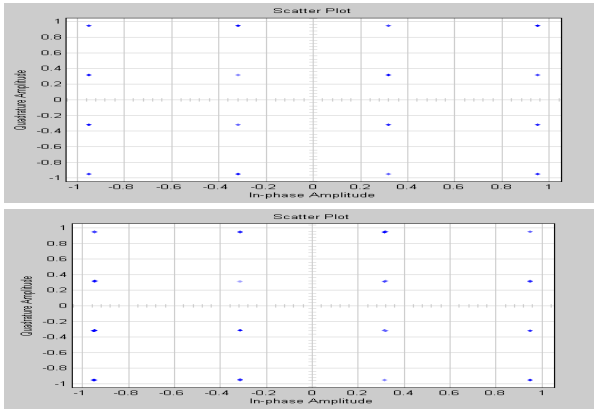


Fig.10 OFDM with 16-QAM; scatter plot for modulator/demodulator, SNR=60 dB

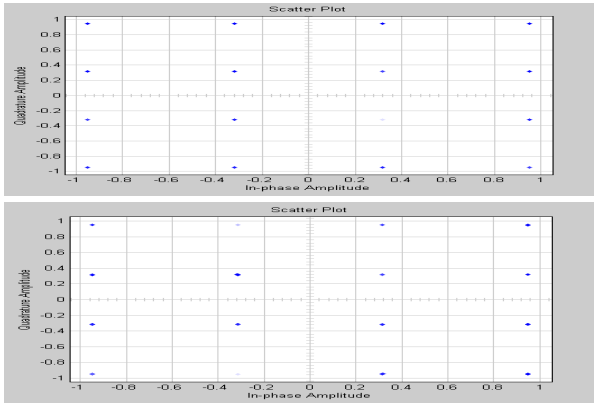


Fig. 11 OFDM with 16-QAM; scatter plot for modulator/demodulator, SNR=70 dB

From the experimental results of this experiment shown in the previous figures we get that the optimum value for the

SNR is 60 dB for minimum scattering in the output of the modulator and demodulator. In the following figures, some adaptive OFDM systems will be observed with its simulation results. The first system is the IEEE802.11a standard:

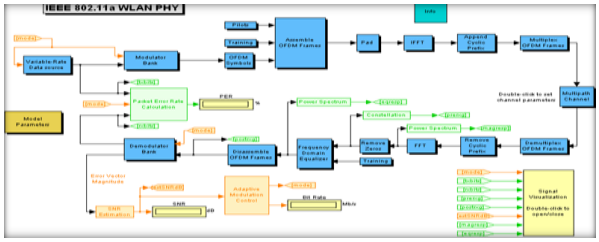


Fig. 12 The block diagram of IEEE 802.11a standard

The simulation results for this system are observed in the following figure;

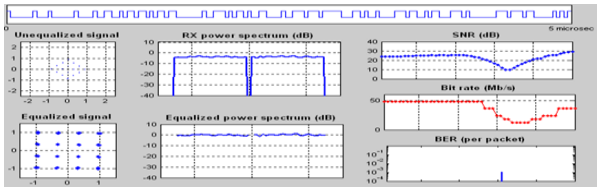


Fig. 13 The simulation results, SNR=60 dB

The second system is the IEEE802.11b standard:

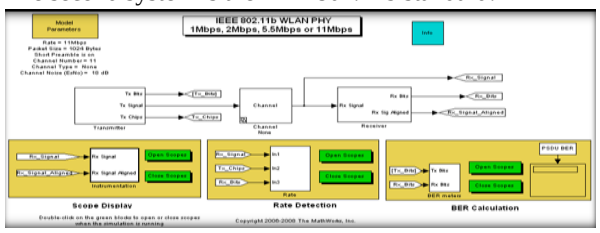


Fig. 14 The block diagram of IEEE802.11b standard

The simulation results for this system are presented in the following figure;

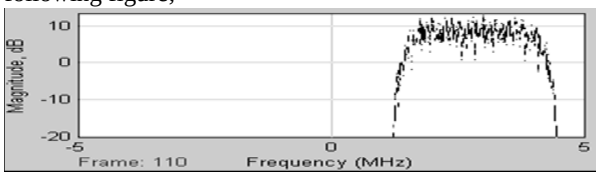


Fig.15 The simulation results, FFT length= 1024 points

The third system is the IEEE802.16a standard:

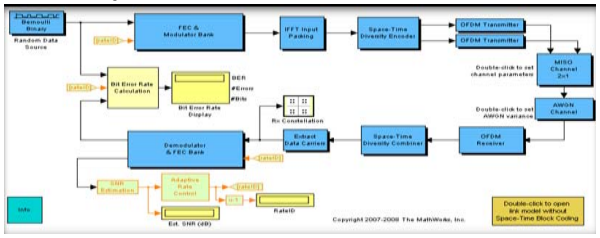
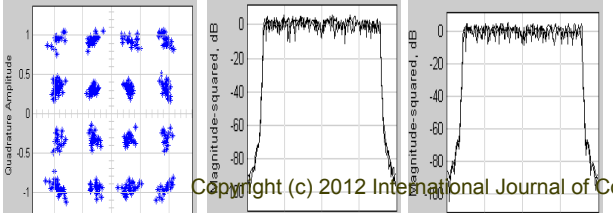


Fig.16 The block diagram of IEEE802.16a standard

The simulation results for this system are shown in the following figures;



From the results of the practical adaptive OFDM systems we get the following; i) As the SNR increases, the noise will decrease but the SNR value can't be increased than specific limit to be practical value. ii) As the length of FFT/IFFT increases, the number of the OFDM channels can be increased but the inter-symbol interference and inter-carrier interference will increase; so the optimum FFT/IFFT length is 1024 points.

5. VHDL EMULATION

In this part the emulation of OFDM elements will be implemented. The implementation process will be carried out using the Mentor Graphics tool FPGA-Advantage 7.2 on the same personal computer presented in the simulated part. The first block of the system is the randomizer which consists of two basic parts; the XOR gate and D-flip flop. The second two blocks together are used for data coding. The third block is the interleaver block for further more coding of the input data to be transmitted. The fourth block is the constellation modulator and in our results we will present some different techniques for constellation mapper as; 2-ASK, 4-ASK, 8-ASK, BPSK, QPSK, and 16-PSK. The next block is the S/P (serial to parallel) converter that is used to convert the data from the serial form to the parallel form to introduce it to IFFT block, and the opposite process in the receiver will be performed using P/S (parallel to serial) converter, the VHDL emulation results for these blocks will be presented in the following figures;

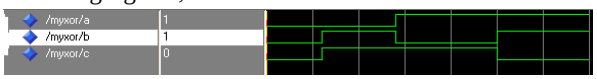


Fig. 18 XOR emulation results

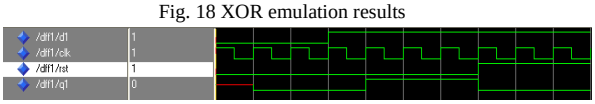


Fig. 19 D-flip flop emulation results

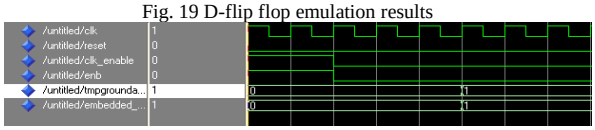


Fig. 20 convolutional encoder & puncher emulation results

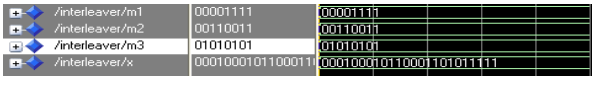


Fig. 21 the interleaver emulation results

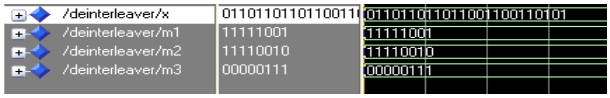


Fig. 22 the deinterleaver emulation results

Fig. 23 2-ASK emulation results

Fig. 24 4-ASK emulation results

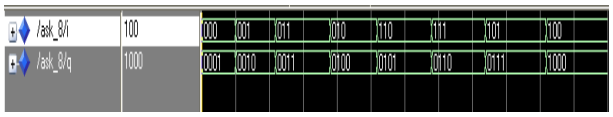


Fig. 25 8-ASK emulation results

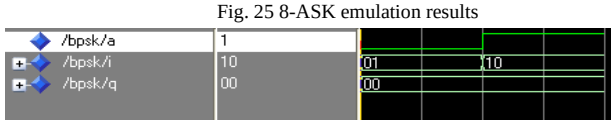


Fig. 26 BPSK emulation results

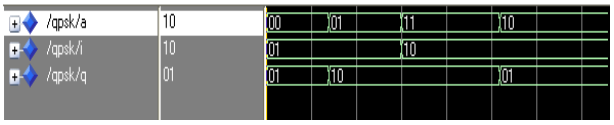


Fig. 27 QPSK emulation results

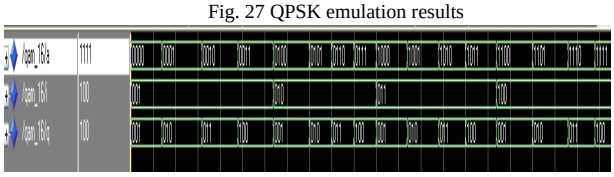


Fig. 28 16-QAM emulation results

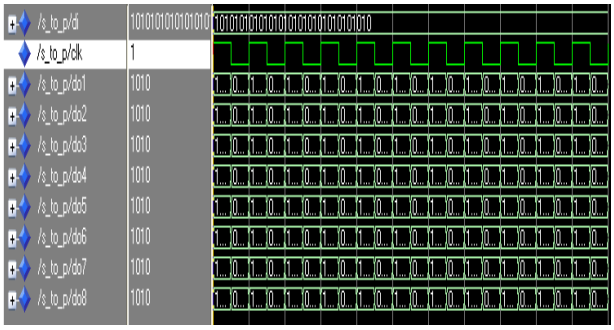


Fig. 29 the S/P emulation results

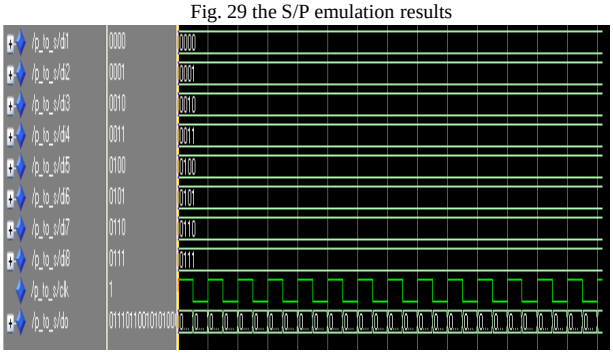


Fig. 30 P/S converter emulation results

The next block is the 8-points IFFT block, and in the receiver the FFT block to reconstruct the carriers. The emulation results for this part will be shown in the following figures;

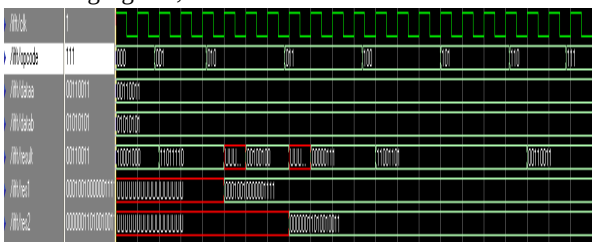


Fig. 31 the IFFT emulation results

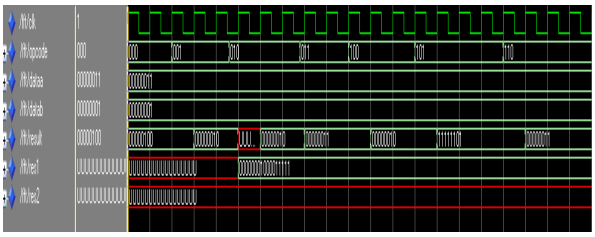


Fig. 32 the FFT emulation results

The last block in the transmitter is the adding of the cyclic prefix block, the opposite for this block is the first block at the receiver (the removing of the cyclic prefix). The emulation results for these blocks will be illustrated in the following figures;

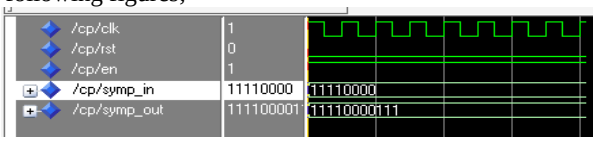


Fig. 33 adding cyclic prefix emulation results

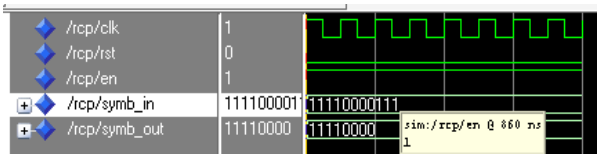


Fig. 34 removing cyclic prefix emulation results

6. Conclusions

As discussed in our paper, the simulation results for OFDM system was observed using MATLAB 2011 program. There were three experiments for that; in the first experiment the changing of FFT/IFFT length with fixed SNR was studied, and in the second experiment the changing of the SNR with fixed FFT/IFFT length has been discussed, in the third experiment the effect of the variation of the SNR over the scatter plot at the demodulator was presented. The main results of our experiments were that the optimum FFT/IFFT length was 1024 points and the best value for the SNR was 60dB; and we get that after this value there is no effect of varying the SNR value. After that the VHDL emulation of OFDM system has been observed using FPGAadv7.2 program, then we could implement this system on Xillinx Spartan 3-A kit.

References

[1] S. J. Vaughan-Nichols, "OFDM: Back to the Wireless Future," IEEE Computer, pp. 19–21, vol.35, issue 12, Dec. 2002.
[2] Steepest Ascent Ltd., *The DSPedia* (www.steepestascent.com), last access Nov. 2011.
[3] M. Serra, J. Ordiex, P. Marti and J. Carrabina, "OFDM Demonstrator: Transmitter" in Proc 7th International OFDM Workshop 2002, Sep 200.
[4] Ma. J. Canet, F. Vicedo, J. Valls and V. Almenar, "Design of a Digital Front-End Transmitter For OFDM-WLAN Systems Using FPGA", Control, Communications and Signal Processing 2004, First International Symposium on, pp: 503–506, 2004.
[5] C. Dick and F. Harris, "FPGA Implementation of an OFDM PHY" Signals, Systems and Computers, 2003. Conference Record of the Thirty-Seventh Asilomar Conference, Vol.1, pp: 905–909, Nov. 2003.
[6] L. de Souza, P. Ryan, J. Crawford, K. Wong, G. Zyner and T. McDermott, "Rapid Prototyping of 802.11 wireless modems", Solid-State Circuits Conference, 2001. Digest of Technical Papers. ISSCC 2001 IEEE International, pp: 339-495, Feb.2001
[7] Y. Kim, H. Jung, H. Ho Lee and K. Rok Cho and F. Harris , "MAC Implementation for IEEE 802.11 Wireless LAN", ATM (ICATM 2001) and High Speed Intelligent Internet Symposium, 2001. Joint 4th IEEE International Conference on, pp. 192–195, Apr. 2001.
[8] Y. Awad, L. H. Crockett and R. W. Stewart, "OFDM TRANSCEIVER FOR IEEE 802.20 STANDARDS".
[9] P. G. Lin, "OFDM simulation in MATLAB", a senior project, faculty of California Polytechnic State University, San Luis Obispo, June 2010.
[10] M. A. Mohamed, "FPGA-BASED DESIGN OF OFDM SYSTEM", the Mediterranean Journal of Computers and Networks, Vol. 7, No. 1, pp: 163-170, 2011.
[11] F. M. Gutierrez, P. L. Gilabert, "Implementation of a Tx/Rx OFDM system in a FPGA," Master thesis, Francisco Martin Gutierrez, April, 30th 2009.
[12] K. A. Kadiran, "Design and implementation of OFDM transmitter and receiver on FPGA hardware", Master thesis, Universiti Teknologi Malaysia, 10 November 2005.
[13] A. Cortés, I. Vélez, I. Zalbide, A. Irizar, and J. F. Sevillano, "An FFT Core for DVB-T/DVB-H Receivers," VLSI Design, vol. 2008, Article ID 610420, 9-pages , 2008.
[14] Z. Sun, X. Liu, and Z. Ji, "The Design of Radix-4 FFT by FPGA," International Symposium on Intelligent Information Technology Application Workshops, 2008, pp.765-768.
[15] Datasheet. September 2008, "Xilinx LogiCore Fast Fourier Transform," Version 4.1, Xilinx Inc. Available: http://www.xilinx.com.
[16] M. Helaoui, S. Boumaiza, A. Ghazel, and F. M. Ghannouchi, "On the RF/DSP design for efficiency of OFDM transmitters," IEEE Trans. Microw. Theory and Tech., vol. 53, no. 7, pp. 2355-2361, Jul. 2005.
[17] N. Balaji, K. Subba Rao, and M. Srinivasa Rao. 2009. " FPGA Implementation of Ternary Pulse Compression Sequences with Superior Merit Factors," NAUN international Journal of Circuits, systems and signal processing. Volume 2, issue 3, pp. 47-54. Available: http://www.naun.org/journals/circuitssystemssignal/
[18] User Guide. January 2009, "Virtex-5 FPGA XtremeDSP Design Considerations," Version3.3, Xilinx Inc. Available: http://www.xilinx.com.
[19] P. L. Gilabert, A. Cesari, G. Montoro, E. Bertran and J. M. Dilhac "Multi Look-Up Table FPGA Implementation of an Adaptive Digital Predistorter for Linearizing RF Power Amplifiers with Memory Effects," IEEE Trans. Microw. Theory and Tech., vol. 56, n? 2, pp. 372 - 384, Feb. 2008
[20]F.B.O. Bartzoudis, N. Pascual-Iserte, A. L'opezBueno, "Design/ Implementation and Testing of a Real Time Mobile WiMA X Testbed Featuring MIMO Technology. In: 6th International ICST Conference Testbed and Research Infrastructures Development of Networks and Communications (Trident Com), Berlin 2010.
[21] Lecture Notes of the Institute for Computer Sciences, Social-Informatics and Telecommunications Engineering (LNICST), Vol. 46, num.5, PP.199-208 (2011).

Biographies

Mohamed Abdel-Azim received the PhD degree in Electronics and Communications Engineering from the Faculty of Engineering-Mansoura University-Egypt by 2006. After that he worked as an assistant professor at the Electronics & Communications engineering department until now. He has 40 publications in various international journals and conferences. His current research interests are in multimedia processing, wireless communication systems, and Field Programmable Gate Array (FPGA) applications.

Mohamed Ismail received the BSC degree in Electronics and Communications Engineering from the Faculty of Engineering-Mansoura University-Egypt by 2007. After that he worked as a demonstrator at the higher institute of engineering and technology of delta-Mansoura-Egypt. His current research interests are in wireless communication systems and Field Programmable Gate Array (FPGA) applications.