Accurate dynamic power model for FPGA based implementations

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Abstract

This paper presents an accurate field programmable gate array (FPGA) of analytical dynamic power models for basic operators at the RTL (Register Transfer Level) level. The models are based on the frequency, the activity rate and the input precision by using the Xpower tool in the presence of the autocorrelation coefficient. The power consumed by the connection between operators was taken into account. We have validated our approach by using the FIR filter computing application in an FPGA Virtex2Pro. The experimental results show that the average accuracy of the model is higher and the maximum reached average error is equal to 10%.

Keywords: *FPGA, dynamic power models, RTL level, autocorrelation.*

1. Introduction and related works

The rapidly advanced technology, the increased integration density and the clock frequency make power consumption more and more important. Furthermore, the mobile applications battery operating time, the production cost and the circuit reliability are so much affected by the power dissipation increase. So, it is very necessary to consider the power-performance trade-offs and to develop appropriate power-aware methodologies and techniques. Power-aware hardware design methods are currently used at several abstraction levels, starting from the physical level up to the behavioral level. It is widely recognized that the greatest power savings can be achieved at the highest levels of a design. Many high level power estimation models were developed in earlier works. An RTL (Register Transfer Level) model was developed in [1]. It considers wire length capacitance and switching activity. These estimates were made even better in [2] by considering short circuit power and leakage power. The high level techniques can be divided into two categories: probabilistic and statistical. Probabilistic techniques [3], [4], [5] are based on input stream to estimate the switching activity of the circuit. The use of probabilities was first used in [6] where a zero delay was assumed and a temporal independence assumption was considered so the transition probabilities are computed using the signal probabilities which are supplied by the user at the inputs and propagated from the inputs to the outputs of the circuit.

Another probabilistic approach was proposed in [7][8], where the transition density measure of circuit activity was introduced and an algorithm was used for propagating the transition density into the circuit. This approach does not take the zero delay assumption but makes only the spatial independence assumption. These techniques are very efficient, but they cannot accurately capture factors like glitch generation and its propagation. While in statistical techniques [9][10][11], the circuit is simulated under randomly generated input patterns and monitoring the power dissipation using simulator. For accurate power estimation, we need to produce a required number of simulated vectors, which are usually high and causes run time problem. To handle this problem, a Monte Carlo simulation technique was presented in [12]. This technique uses input vectors that are randomly generated and the power dissipation is computed. Those samples combined with previous power samples are required to determine whether the entire process needs to be repeated in order to satisfy a given criteria. A survey sampling perspective was addressed in [13]. The sequence vectors were provided to estimate power dissipation of a given circuit with certain statistical constraints such as confidence level and error. This technique divides the vectors sequence into consecutive vectors, to constitute the population of the survey. The average power is estimated by simulating the circuit by a large number of samples drawn from the population [14]. For better accuracy, numerous power macromodeling techniques [15][16], have been introduced. In [17], the authors used analytical approach without considering temporal correlation. Some other basic power macro models [18][19][20] located at the RTL level while exploiting the low level characteristics have been explored. These models depend on the probability, the transition density, the spatial and temporal correlations taking into account the spatial independence between signals. In this case the effect of convergence paths is ignored whereas models accuracy decreases.

We present in this work analytical power models related to based LUTS arithmetic operators (adder, multiplier) and a

bloc multiplier function to the frequency F, the activity rate α and the precision w in the presence of an autocorrelation coefficient. We have introduced, also, the power consumed by the interconnections between operators, so the global application model includes the power consumed by the whole operators and those consumed by the interconnections between them. The validation of our models was performed on a FIR filter application.

This paper is organized as following. In the first part we introduce the problem and describe some related works. In the second one, we describe the mathematical operator's power models and the interconnections power between operators. The results are reported in the third part. Finally, we conclude and explore our future works.

2. Dynamic power estimation methodology

It has been shown that dynamic power consumption in arithmetic components is affected to a greater extent by autocorrelation than by crosscorrelation [21][22].Therefore, we have developed a signal generator similar to [21], which generates two signals with variable autocorrelations coefficient and variances from two zero mean gauss signals. All results are obtained for a positive autocorrelation values belong to the interval [0, 0.999] and a variance value equal to 0.5.

The developed models are obtained by using the Xilinx Xpower tool, in the presence of autocorrelation coefficient and with an examination of the glitches effect on power consumption. The models are based on the frequency, the input precision and the activity rate. The following figure describes the operator power estimation methodology (Fig.1).

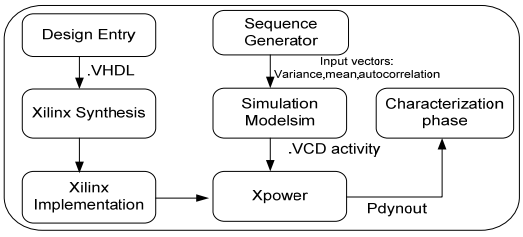

Fig.1 Estimation methodology description

For each input sequence vector, we calculate its activity_rate (activity_inputs) as the average number of transitions from 0→1 and 1→0 of each bit b_i of the vector l and then we propagate these sequences from the input to the output in order to evaluate the application activity rate. The average activity is calculated by the basic formula as follows:

$$average\_activity = \frac{1}{w} \times \sum_{w} \left(\frac{1}{L-1} \times \sum_{l=1}^{L} \left(tr_{b_i(l) \to b_i(l+1)}(0 \to 1) + tr_{b_i(l) \to b_i(l+1)}(1 \to 0) \right) \right) \quad (1)$$

Where L is the number of vectors sequence and w is the precision of each vector l; $1 \leq b_i \leq w$

The coefficients of the various models are determined by the nonlinear approximation method based on the Levenberg-Marquardt algorithm [23] which generates an optimal solution after n iteration with a 10^{-4} error tolerance. The superposition of the measurement curve and the model for each operator enables us to evaluate the average error by the following formula:

$$Error\ (\%) = \frac{P_{dyn}(Xpower) - P_{dyn}(model)}{P_{dyn}(Xpower)} \times 100 \quad (2)$$

2.1 Basic Operator models

The static power is assumed to be invariant in function of the activity design because implemented circuits are small and the static power increase is negligible. We have reported in this part, the measured power by using the Xpower tool which is described by the curve marked by circles. The curve marked by triangles represents the estimated mathematical model, whereas the error between the two models is illustrated by the curve marked by squares. All the tests are done on Virtex2Pro (XC2VP4).

2.1.1. Adder model

In order to expand the generic adder power model, we have varied the frequency F, the input activity in presence of the autocorrelation coefficient and the input precision w from 8bit, 16 bit, 24 bit to 32 bit (Table 1). The following table and figure illustrate the power variation and report a max reached error of 0.22% between the measured Pdyn(Xpower) and the estimated power, which demonstrates the accuracy of our adder model.

Table 1: Performances of the generic adder model

activity _input	*F (Mhz)*	*ρ*	*w*	*activity _ rate*	P_{dyn} *Xpower (mw)*	P_{dyn} *(estimated model) (mw)*	*Error (%)*
0.474	25	0.4	8	0.487	18	17.96	0.220
0.486	50	0.6	16	0.501	69	68.98	0.028
0.467	75	0.8	24	0.312	95	94.97	0.031
0.420	100	0.99	32	0.200	112	111.93	0.062

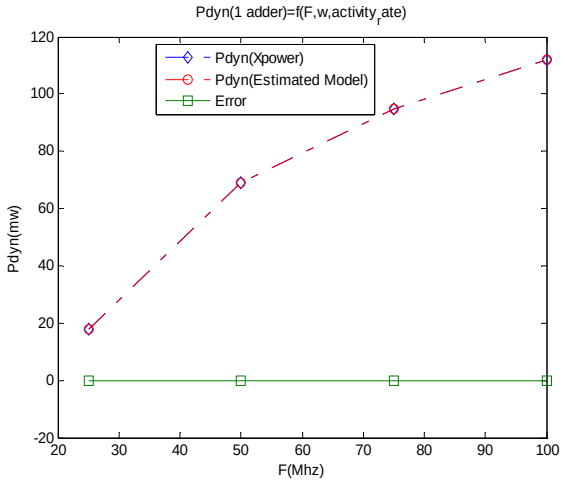

Fig.2 Adder Dynamic power variation

The adder dynamic power model is illustrated by this equation function to the frequency, the precision and the activity rate:

$$P_{dyn}(Adder)(F,w,\alpha) = a_1 \times F \times \alpha \times w + b_1 \times F + c_1 \times \alpha + d_1 \times w + e_1 \qquad (3)$$

2.1.2. Based Luts multiplier model

The same measurement has been done for the based luts multiplier. The figure bellow illustrates the dynamic power variation and it demonstrates a max reached error of 0.1 % between the two powers (Fig. 3).

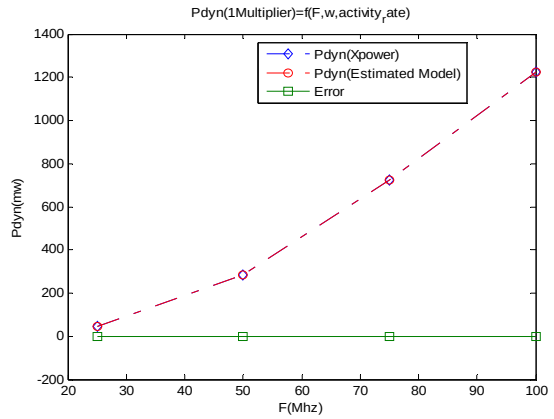

Fig.3 Based luts multiplier dynamic power variation

The model can be approximated by this formula:

$$P_{dyn}(Multiplier)(F,w,\alpha) = a_6 \times F \times \alpha \times w^2 + b_6 \times F + c_6 \times \alpha + d_6 \times w^2 + e_6 \qquad (4)$$

2.1.3. Block multiplier model

The following figure (Fig. 4) describes the power variation when we use the DSP block (multiplier block).We outline a max reached error of 0.15% between the two power values. The analytical model can be approximated by this formula:

$$P_{dyn}(Multiplier)(F,w,\alpha) = a_7 \times F \times \alpha \times w^2 + b_7 \times F + c_7 \times \alpha + d_7 \times w^2 + e_7 \qquad (5)$$

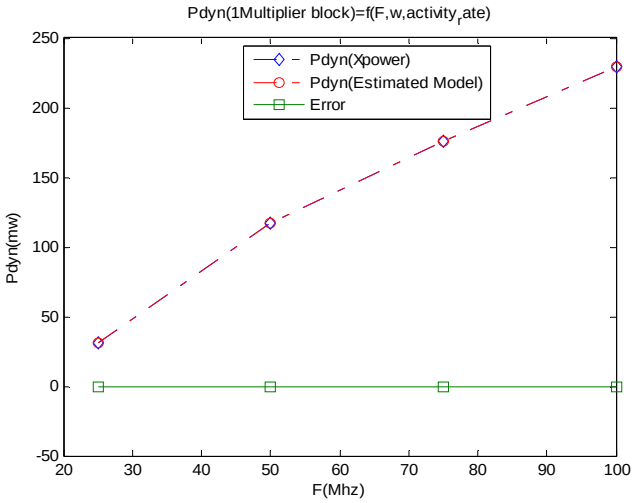

Fig.4 Block multiplier dynamic power variation

We present in this part the dynamic power components models. By using the Xpower tool, the dynamic power model is the sum of four power components regrouped into two cathegory: a first one which depends on the application surface and it includes the logic, the clock and the signal power and a second one independent on surface which is the input/output (I/O) power. The figure bellow describes the variation of input/output power function to the I/O number for the adder and the based Luts multiplier (Fig. 5).

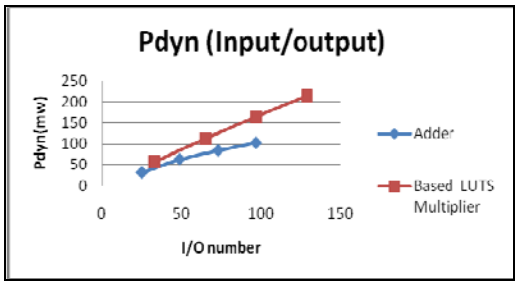

Fig.5 Variation of input/output power

The I/O power variation is modeled by the equation below for a fixed frequency to 100 MHz and in presence of the autocorrelation coefficient. The max reached errors are respectively 1.31% for the I/O adder model and 1.41% for the I/O multiplier model.

$$Pdyn\ (I/O) = N_{I/O}(a_2 \times \rho + b_2) + \frac{c_2}{\rho^2} + d_2 \qquad (6)$$

Although the variation of Ptotal(operator), Pclk, Plogic and Psignal function to the slices number for the adder and multiplier are reported in figure6.

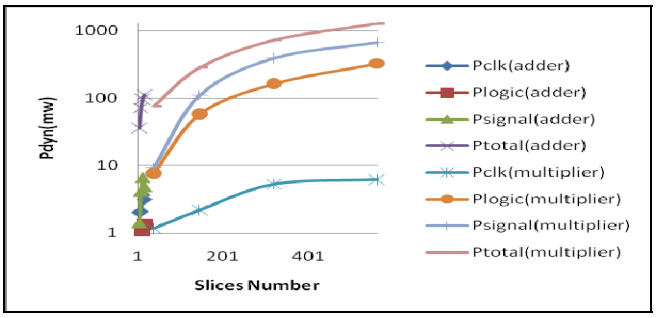

Fig. 6 The variation of Ptotal, Pclk, Plogic and Psignal related to the adder and multiplier operators function to the slices number

The components dynamic power models of adder and multiplier are described by equations as follow. The max reached errors are respectively 2.54% for Plogic(adder), 0.1% for Psignal(adder), 0.25% for Pclk(adder), 1.7% for Plogic(multiplier), 0.19% for Pclk(multiplier) and 2.78% for the Psignal (multiplier).

$$Pdyn\ (\log\ ic) = Slices\ \times (a_3 \times \rho + b_3) + c_3 \times \rho + d_3 \quad (7)$$

$$Pdyn\ (clk) = Slices\ \times (a_4 \times \rho + b_4) + \frac{c_4}{\rho} + d_4 \quad (8)$$

$$Pdyn\ (signal) = Slices\ \times (a_5 \times \rho + b_5) + \frac{c_5}{\rho^2} + d_5 \quad (9)$$

The table (Table2) summarizes the different coefficients power models for the adder and the multipliers (based luts and block):

Table 2: Power models coefficients

Pdyn	$a_1,a_2,a_3,a_4,a_5,a_6,a_7$	$b_1,b_2,b_3,b_4,b_5,b_6,b_7$	$c_1,c_2,c_3,c_4,c_5,c_6,c_7$	$d_1,d_2,d_3,d_4,d_5,d_6,d_7$	e_1,e_6,e_7
Padder	0.1347	0.2937	28.1042	0.288	-18.48
PI/O (adder)	-0.628	1.6731	-0.7966	0.8841	-
PLogic (adder)	-0.0637	0.1193	0.703	-0.2652	-
PClock (adder)	-3 .7192	6.9059	18 .795	-66.6605	-
PSignal (adder)	-4.4757	7.0724	3.2391	-39.963	-
Pmultiplier	0.1301	-5.6281	-299.1913	-1.576	329.77
PI/O (multiplier)	-0.065	1.7272	1.0174	1.0664	-
PLogic (multiplier)	0.3793	0.2197	-1.2991	-5.6058	-
PClock (multiplier)	-0.1071	0.1869	-57.2408	18.7246	-
PSignal (multiplier)	-0.0038	1.219	0.1383	2.4051	-
P Block multiplier	0.0043	4.6035	-67.1608	-0.2931	-32.33

2.2. Interconnection power estimation

The interconnections consume an important part of the application global dynamic power [24]. It represents an error source when considering the total application power as the sum of theirs operator's power models. In this work, we model the power consumed by the interconnection part and we add it to the global model to be closer to the real power model. Considering as example, an application E(s=a×b+d) consisting of two operators organized as mentioned in Figure 7, for which we analyze its dynamic power model in the following part.

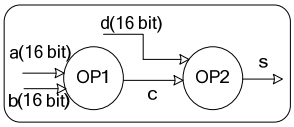

Fig.7 Description of the application E architecture

The figure bellow (Fig.8) illustrates the gap between the application measured power and the estimated one while adopting the operator models. This gap is due to the additional connections between the two operators. The difference between the two power models (green curve) represents the power consumed by the connection C.

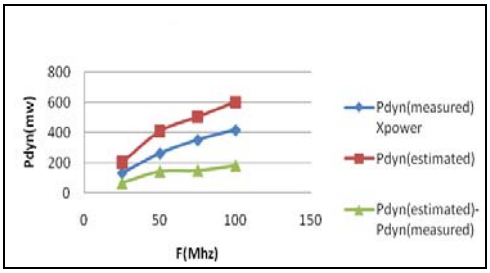

Fig.8 Variation of the application E measured and estimated dynamic power

Several measures showed that connection C power can be identified according to two cases:

- When the two operators are similar then:

$$P_{dyn}(connection\ C) = 2 \times P_{dyn}(operator) - P_{dyn}(2\ series\ operator) \quad (10)$$

- When the operators are heterogeneous, the connection C power value is almost equivalent in both architectures: Arch1 formed by an adder (16 bit) placed in series with a multiplier (16*16) bit or an Arch2 formed by a multiplier(16*16) bit placed in series with an adder(16 bit). The following table (Table 3), illustrates the variation of slices number

and the power of connection C when all the inputs are not correlated (ρ=0).

Table 3: A comparison between connection C power for Arch1 and Arch2

F (Mhz)	*Slices Arch1*	*Pdyn Arch1*	*Pdyn Connection (C) (Arch1)*	*Slices Arch2*	*P_{dyn} Arch2*	*Pdyn Connection (C) Arch2*
25	178	59	115	108	60	114
50		119	228		114	233
100		138	373		169	342

3. Results

To validate the operator's power models, we have chosen an application of a FIR filter which its architecture is described by figure 9 and its surface performance is reported in table 4.

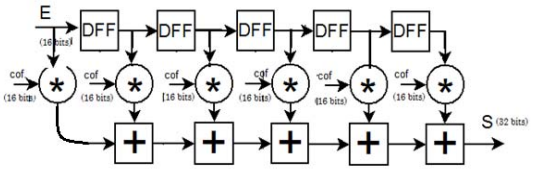

Fig. 9 Description of the FIR architecture

Table 4: The FIR filter surface performances

Slices Number	*Luts*	*IOBs*	*Occupation rate (%)*
1016	1864	65	33

The estimated FIR dynamic power is computed according to the equation (11), with (N_1=6: number of multiplier operators, N_2=5: number of adder operators, β_1=6 and β_2=4).

$$P_{dyn}(estimated) = N_1 \times P_{dyn}(Multiplier) + N_2 \times P_{dyn}(Adder) - P_{dyn}connections \quad (11)$$

Where:

$$P_{dyn}(connections) = \beta_1 \times P_{dyn}connection(multiplier) + \beta_2 \times P_{dyn}connection(adder) \quad (12)$$

β_1, β_2: number of corresponding connections.

The table as below (Table 5) report a comparison between the measured Xpower dynamic power Pdyn1 and our estimated dynamic power model Pdyn2 while adopting the operators models and the interconnection power model for variable frequencies, not correlated inputs (ρ=0) and fully correlated (ρ=0.999) .

Table 5: FIR power consumption performances

ρ	*F(Mhz)*	*Pdyn1 (mw)*	*Pdyn2 (Model)*	*Abs Error (%)*
0	25	686	761.87	11.06
	50	897	987.05	10.04
	75	1065	1159.081	9.26
	100	1324	1435.87	8.45
0.999	25	478	526.89	10.22
	50	545	597.37	9.60
	75	790	854.14	8.12
	100	980	1053	7.44

The table 5 outlines an average error of 10.37% between the measured and estimated model which justifies the accuracy of our models.

4. Conclusion

We have presented in this paper the mathematical dynamic power models for arithmetic operators (adder, multiplier and block multiplier) in function to the frequency, activity rate and precision in presence of the autocorrelation coefficient in Virtex2Pro FPGA. We have presented also the connection dynamic power model between operators. Finally we have validated our models on a FIR filter application and we have outlined an average error of 10% between the two power models. We are currently working to enhance the library by the mathematical power models of the most current IPs, and to develop others methods to estimate and to control the glitches power.

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