A High Performance Architecture for 3D Wavelet Transform

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Abstract

Discrete Wavelet Transform (DWT) is attracted great deal of attention and used in various image, video and signal processing applications. Even though lifting scheme is proposed to reduce the computational load of DWT, traditional hardware solutions based on lifting scheme for DWT suffer from high critical path and computational resources. Flipping structure has been proposed to resolve these problems in the lifting based hardware implementations for DWT. In this paper we propose a pipeline architecture based on flipping structure for 3D DWT. The proposed architecture has lower critical path and computational resources compared to the other proposed hardwares for 3D DWT in the literature. Moreover, the proposed architecture can be used to implement 1D and 2D DWT besides the 3D DWT.

Keywords: *3D Wavelet Transform, Computational resources, Critical path, Flipping Scheme, Lifting Scheme.*

1. Introduction

3D DWT has been used in various image and video compression and processing applications. Encoding volumetric data sets produced by various 3D image acquisition devices such as computed tomography (CT), position emission tomography (PET) and magnetic resonance imaging (MRI) are a number of 3D DWT applications. Scalable video coding and noise reduction between frames of a video are the applications that we can name for 3D DWT in the field of video coding and processing. DWT is one of the most computationally intensive parts in these image and video coding applications. Even though lifting scheme [1],[2] is proposed to reduce the computational load of DWT, it still takes relatively large portion of coding time in the image and video coding process. As a result hardware realization of DWT has been widely considered as a solution to reduce the coding time in the real time applications [3]. Nevertheless, traditional lifting based hardware realizations for DWT suffer from high critical path and hardware overhead. Flipping structure has been introduced to resolve these problems [4]. Although, there are proposed solutions for 1D and 2D flipping DWT [5],[6] and also hardware solutions for 3D lifting based DWT [7]-[9], there is not proposed any high performance architecture for 3D DWT based on flipping structure, as much as we know.

In this paper we propose a high efficiency parallel architecture for hardware implementation of 3D DWT based on flipping structure. The proposed architecture reduces the critical path latency and the number of processing units compared to the traditional lifting based 3D DWT architectures. Moreover, the proposed architecture can be used to produce 1D and 2D DWT besides 3D DWT. The rest of paper is organized as follows. In section 2, we introduce our proposed architecture followed by simulation results in section 3. The concluding remarks are given in section 4.

2. Proposed Architecture

The lifting scheme for WT by using 9/7 Debauchee's filter is performed as follows

$$s_i^0 = x_{2i} \tag{1}$$

$$d_i^0 = x_{2i+1} \tag{2}$$

$$d_i^1 = a \times d_i^0 + s_i^0 + s_{i+1}^0 \tag{3}$$

$$s_i^1 = b \times s_i^0 + d_i^1 + d_{i-1}^1 \tag{4}$$

$$d_i^2 = c \times d_i^1 + s_i^1 + s_{i+1}^1 \tag{5}$$

$$s_i^2 = d \times s_i^1 + d_i^2 + d_{i-1}^2 \tag{6}$$

$$s_i = k_1 \times s_i^2 \tag{7}$$

$$d_i = k_2 \times d_i^2 \tag{8}$$

where x_{2i} and x_{2i+1} are even and odd input elements, respectively and $a = 1/\alpha$, $b = 1/\alpha\beta$, $c = 1/\beta\gamma$,

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$d = 1/\gamma\delta$, $k_1 = \alpha\beta\gamma\delta\zeta$ and $k_2 = \alpha\beta\gamma/\zeta$ and $\alpha, \beta, \gamma, \delta$ and ζ are the coefficients employed in the lifting scheme and listed in Table 1, s_i^0 and d_i^0 represent the input odd and even parts respectively, s_i^n and d_i^n (n=1,2) represent the intermediate value obtained in the lifting process, and s_i and d_i represent the low pass and high pass parts of the output signals, respectively. k_1 and k_2 are also known as k_L and k_H, respectively. In fact in flipping scheme there will be a final scaling stage by factors k_L and k_H which will be applied in the last filtering step.

Table 1: Lifting Scheme Parameters

Parameter	Approximate Value
α	-1.586134342059924
β	-0.052980118572961
γ	0.882911075530934
δ	0.443506852043971
ζ	1.230174104914001

In flipping scheme from one side (3) is merged with (4) and on the other side (5) is merged with (6) resulting the outputs in stage 2 as [4]:

$$s_i^1 = bs_i^0 + d_i^1 + d_{i-1}^1 = bs_i^0 + ad_i^0 + s_i^0 + s_{i+1}^0 + ad_{i-1}^0 + s_{i-1}^0 + s_i^0 \quad (9)$$

$$s_i^2 = ds_i^1 + d_i^2 + d_{i-1}^2 = ds_i^1 + cd_i^1 + s_i^1 + s_{i+1}^1 + cd_i^1 + s_{i-1}^1 + s_i^1 \quad (10)$$

In flipping structure is similar to the basic lifting structure except that the scaling is performed in different order. For example in the first stage of lifting scheme the scaling is performed as shown in Fig. 1.a. While the scaling in flipping structured is as shown in Fig. 1.b. Comparing Fig. 1.a and 1.b indicates that in flipping structure the number of the multipliers is decreased compared to original lifting scheme.

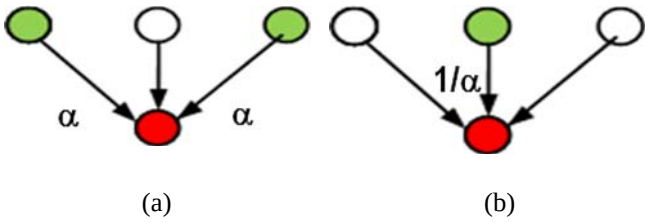

Fig. 1. Scaling methods in original lifting (a) and flipping (b)

The following data path in Fig. 2 is introduced by Hao et al. [6] to implement (9) and (10). This data path employs one multiplier and two adders to produce one output per clock. This data path has the advantage of lower critical path over the traditional lifting scheme for WT. The critical path in the flipping scheme is one multiplier ™ in contrast to the critical path of flipping scheme which includes one multiplier (Tm) and two adders (Ta).

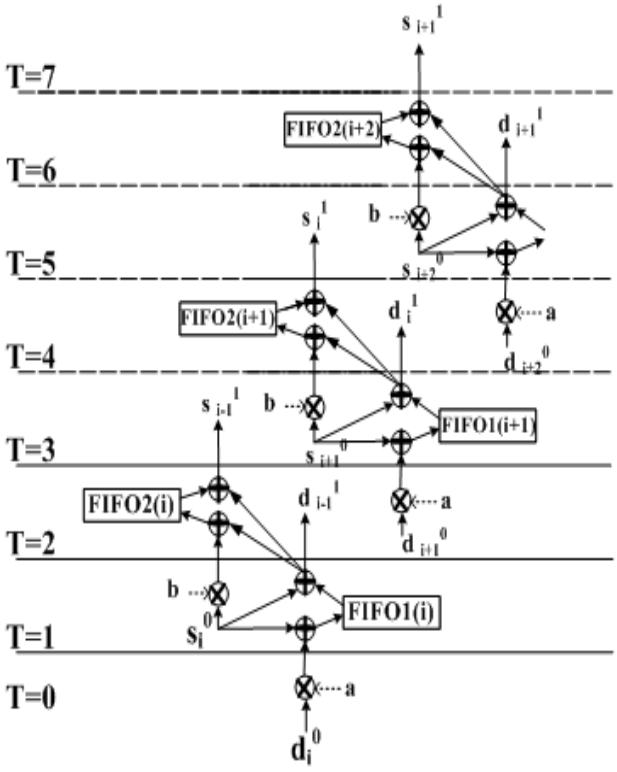

Fig. 2. Datapath for realization of the first stage of flipping scheme [6]

Hao et al. [6] introduced the hardware in Fig. 3 to implement the 1D WT according to flipping scheme. We refer to the architecture in Fig.2 as “basic unit” hereafter. This architecture is the basic building block for the 1D and 2D flipping based DWT hardwares.

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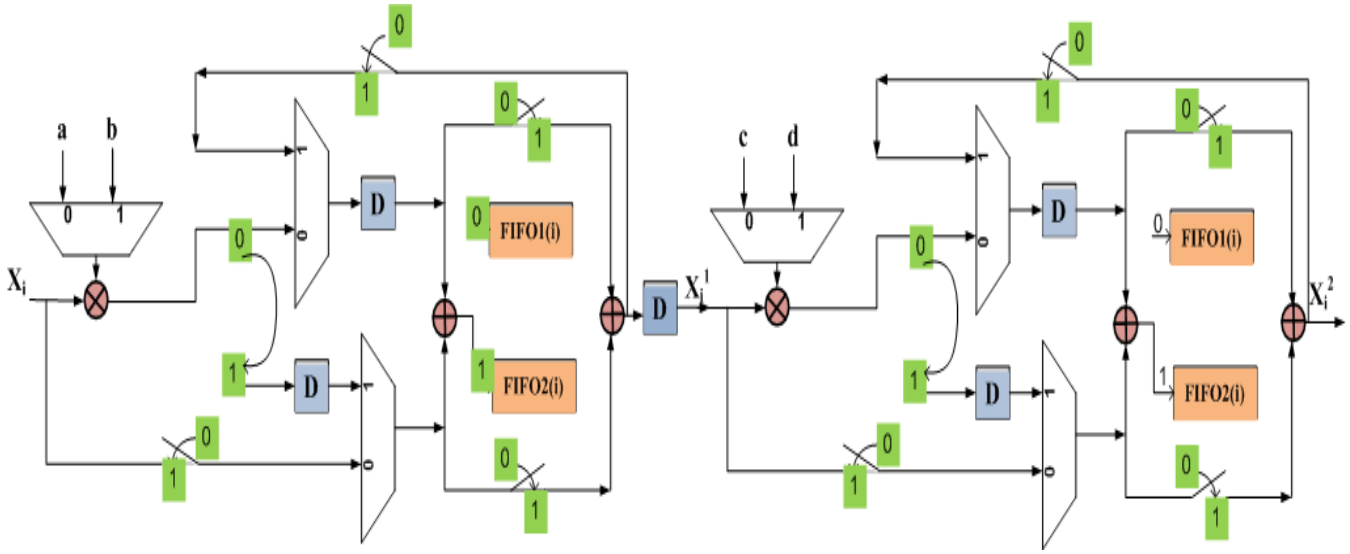

Fig. 3. Proposed architecture in [6] to implement 1D WT

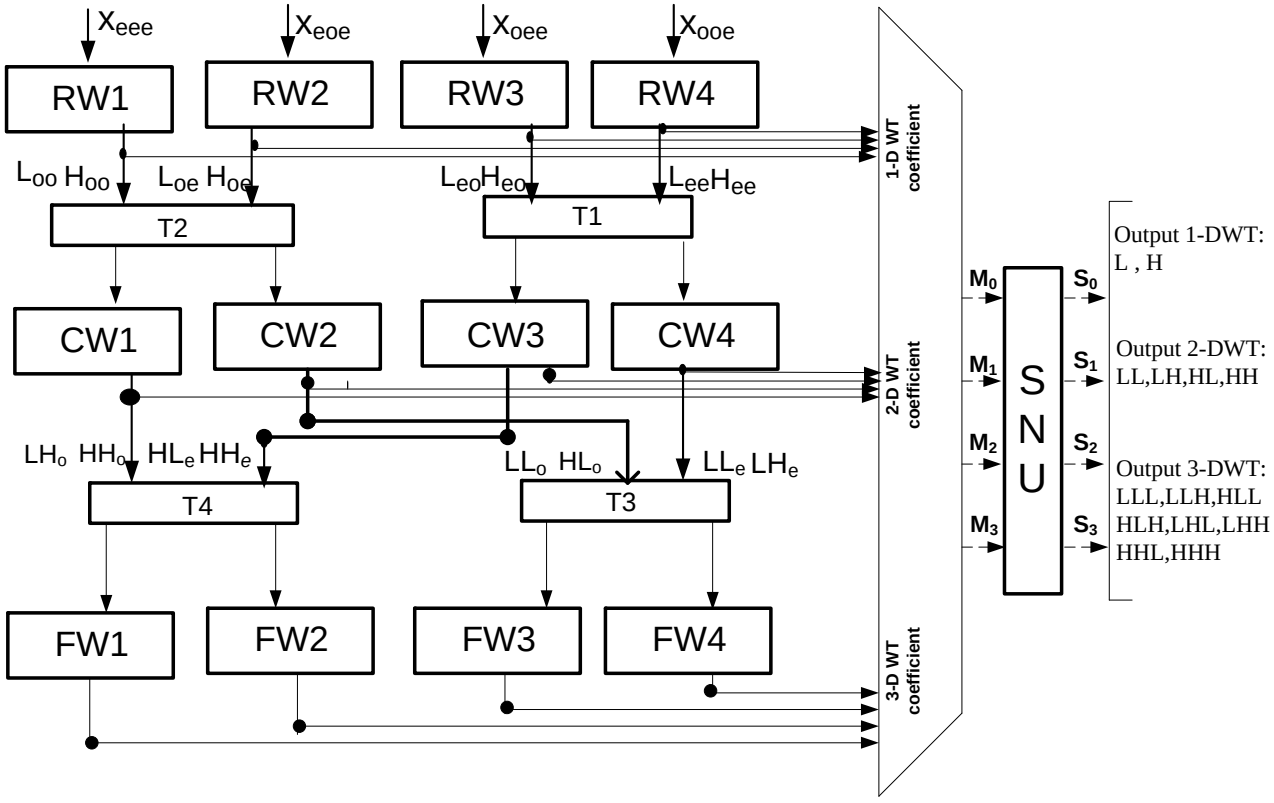

Fig. 4. Proposed parallel and pipelined architecture to implement 3D WT

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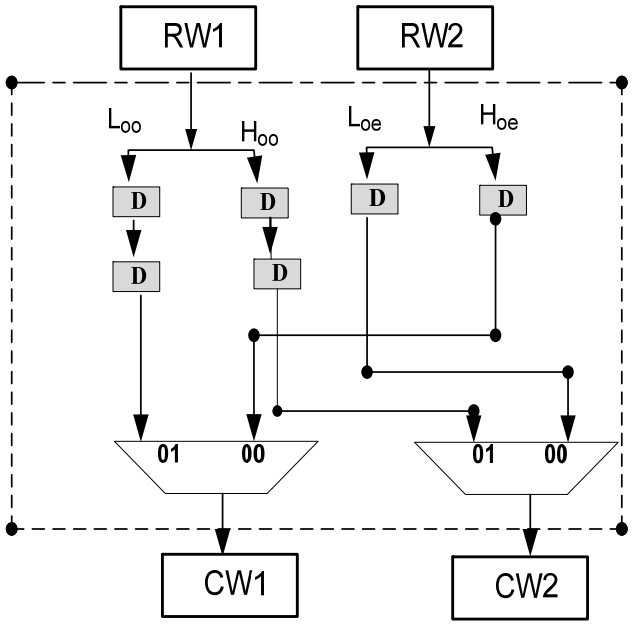

Fig. 5. The Transpose Unit

We have proposed a parallel and pipelined flipping structure for 3D DWT by using the basic transform unit given in Fig. 3. Fig. 4 indicates the proposed architecture. It consists of 12 one dimensional basic transform units in row, column and time stages, four transpose modules and one scaling unit (SNU). The first transform stage (row transform) employs four basic transform units each one has four inner registers. As a result it requires eight multipliers, 16 adders and 16 registers. The first stage gets four inputs and produces 1D DWT of the inputs at the output. The outputs are applied to T1 and T2 transpose units to come to the appropriate order for the next transform stage. The architectures of the entire transpose units in Fig. 4 are similar and Fig. 5 indicates the schematic of transpose unit T1. Fig. 5 indicates that each transpose unit consists of six delay elements and two multiplexers.

Second stage performs the next 1D transform on its inputs and produces the 2D DWT of the initial image coefficients. The number of basic transform units in the second stage is similar to the first stage but the second stage requires 16×M registers for an N×M×F image sequence. The third transform stage receives the outputs of the second stage in the corrected order via T3 and T4 transpose modules. The number of the basic transform units in this stage is the same as the previous stages, but the number of registers increases to 8×M×N registers for an N×M×F image sequence.

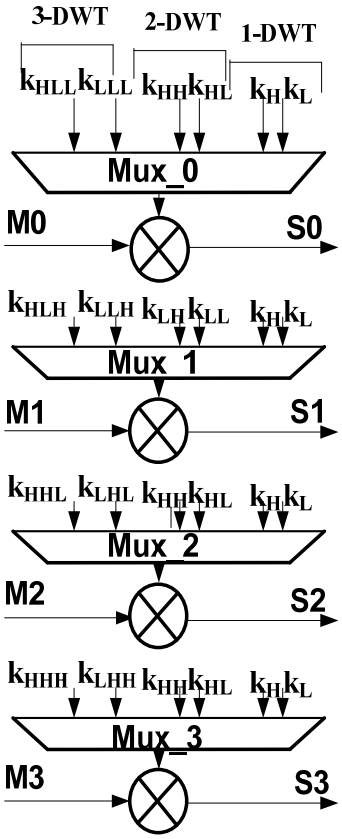

Fig. 6. The schematic diagram of SNU

In the final stage, SNU unit scales the outputs of first, second or third stage, scaling them for 1D, 2D or 3D DWT, respectively. The schematic diagram of SNU is shown in Fig. 6. In the case of 1D transform, that is inputs from first transform stage, the even coefficients are scaled by k_L and the odd coefficients are scaled by k_H. For the inputs from the second transform stage. M0 and M2 are derived from odd rows and are scaled by k_{HH} and k_{HL}, where as M1 and M3 are come from even rows and should be scaled by k_{LL} and k_{LH} in order to generate 2D DWT coefficients. In the case of 3D DWT the inputs of SNU are come from the third transform stage. The inputs to M0 (even colomn and row), M1 (even row and odd colomn), M2 (even colomn and odd row) and M3 (odd colomn and row) are respectively scaled by (k_{LLL}, k_{HLL}), (k_{LLH}, k_{HLH}), (k_{LHL}, k_{HHL}) and (k_{LHH}, k_{HHH}) to produce the final 3D DWT coefficients.

k_L and k_H are the coefficients used in the 1D DWT. k_{ab} (where a and b are H or L) are the coefficients used in 2D DWT and are equal to $k_a \times k_b$. On the other hand, k_{abc} (where a, b and c are H or L) are 3D DWT scaling coefficients and are equal to $k_a \times k_b \times k_c$.

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Table 2: Comparing the Architectures for 3D WT

Architecture	Multiplier	Adder	Buffer memory	Critical path	# of outputs per clock	Type of DWT
Dai[8]	96	72	4(N+2)M	T_m+2T_a	4	Lifting
Das[9]	48	40	$3.5N^2+4N$	T_m+2T_a	4	Lifting
Xiong[7]	56	96	$5.5N^2+8N$	T_m+2T_a	8	Lifting
Porposed	28	48	8(2N+MN)	T_m	4	Flipping

3. Simulation Results

The proposed architecture is implemented by VHDL and applied to an image sequence including six 352×288 images. The hardware simulation results verified by the results derived from the software in C language for flipping based 3D DWT. The specifications of the proposed architecture and 3 previously proposed architectures for 3D DWT are listed in Table 2.

The simulation results indicate that the critical path of the proposed architecture is equal to one multiplier delay (Tm) while the critical path delay for the rest of the architectures increases by two adders' delay (2Ta) besides one multiplier delay (Tm). Moreover the proposed architecture requires 28 multipliers and 48 adders which are totally less than the architecture with minimum processing units in Table II that is proposed by Das et al [9]. Besides the aforementioned advantages the proposed architecture can be used to generate 1D and 2D DWT coefficients as well.

4. Conclusions

In this paper we introduce a parallel and pipelined architecture based on flipping structure for 3D DWT. The proposed architecture requires less processing units compared to the other tested architectures. Furthermore the proposed architecture reduces the critical path of the other proposed architectures from 2Ta+Tm to only one Tm.

Moreover, the 1D and 2D DWT coefficients can be realized by the proposed architecture besides the 3D DWT. Therefore, the proposed architecture can be used in the real time 1D, 2D and 3D DWT applications which require high performance and throughput along with low computational resources and critical path.

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