Loss-Aware Router Design Approach for Dimension- Ordered Routing Algorithms in Photonic Networks-on-Chip

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Abstract

Photonic-Network-on-chip (PNoC) has been proposed as a promising solution for the communication infrastructure of Chip Multiprocessors (CMPs) and as a solution to overcome the constraints in traditional NoCs. Photonic NoCs provide the opportunity of increasing both the bandwidth and the number of cores significantly, and can improve performance and the cost parameters of CMPs. In this paper, a designing approach for a photonic router has been proposed in order to reduce insertion loss in photonic NoCs, which can in turn increase network throughput, since it uses more parallel wavelengths. It has also led to the design of a router structure exclusively for XY routing algorithm. The proposed router shows an improvement of up to 52% in insertion loss, when compared to other proposed routers.

Keywords: *Photonic NoCs, Insertion Loss, XY Routing Algorithm, Non-blocking*

1. Introduction

The increase of processing requirement for a variety of applications in the last decade and the restrictions in designing single-core processors with high computing power have both led the designers to switch to multi-core chips. However, as the CMPs become more complex, the communication bus begin to act as a bottleneck in multi-core chips [1]. Indeed, due to the limitations of bus structure, Network-on-Chips are proposed as a strategy to increase the number of cores [2].

However, as the number of cores grow, the common on-chip electrical communications cannot meet the requirements of advanced systems due to their low bandwidth and high power consumption [3]. Fortunately, recent researches in the field of fabricating photonic silicon technologies compatible with CMOS [4] have provided the opportunity to build a suitable infrastructure for designing PNoCs as an appropriate solution In order to overcome the issues of future NoCs [5,6]. One of the advantages of photonic NoCs in Nano-scale era is the high bandwidth of the network [7]. Also, its performance can be increased noticeably by using Wavelength-Division-Multiplexing (WDM) method [12]. In addition, since waveguides are independent of distance, and data-rate per bit does not impact power consumption in waveguides and photonic switches [9], power consumption in such networks is desirable.

During the recent years, different designs of photonic networks have been proposed and most of them possess a significant improvement compared to their electric counterparts [10]. Photonic routers serve as one of the key components of photonic NoCs, and they are considered important when defining performance and cost parameters such as insertion loss, power dissipation and throughput. In this paper we have proposed a new method to design a non-blocking photonic router in which photonic signals have a lower insertion loss and its power consumption is negligibly reduced compared to other proposed routers when using XY routing algorithm. The proposed router is evaluated in a photonic network with hybrid Mesh structure.

The rest of the paper is organized as follows: In section II an overview of some proposed router structures is mentioned. Section III is dedicated to the photonic network topology used in this paper and the description of the required components in photonic networks. In section III we will explain our design approach which has led to the introduction of a new router structure. In section IV, simulation results are evaluated and showing improvements in performance and cost parameters in the proposed router in comparison with other routers. Finally, section V is dedicated to conclusion and future works.

2. Related work

Since the introduction of photonic Network-on-Chips as an effective solution by Shacham et al. [11], two main categories of PNoCs have also emerged: Hybrid and Wavelength-Routed structures [9]. Each of them have been used and developed during the recent years. Many structures have been proposed based on the Wavelength-Routed structure, such as CORONA network, introduced by Vantrease et al. [21], FIREFLY network, proposed by

Pan et al. [10] and CLOS network, which was the result of Joshi et al. researches [22]. As we will explain later, Hybrid structures have been developed in some other papers as well [6_7, 10_16].

In the field of Hybrid Networks, the first Photonic NoC router structure was proposed by Shacham et al. [11] in 2007, with the capability of being used in Mesh and Torus topologies. However, the main drawback of the structure was the existence of blocking [18], which could have negative effect on router's performance [18]. Thereafter, Shacham et al. proposed a new router which was non-blocking [14], which was used in Torus topology. Later, J. Chan et al. [19] introduced two new non-blocking router structures, having the possibility of being exploited in both Mesh [12] and Torus [14] topologies. It is worth mentioning that X. Yin et al. [16] have also used this router for Honey Comb topology. Despite using general fully connected routers in many papers, some others have used customized routers as their proposed structures. For instance we can refer to [17] by koohi et al. in which Spidergon topology has been exploited based on their contention-free router. We can also refer to [15] by G. Huaxi et al. in which a customized router for Fat-Tree topology has been introduced.

It is worth noting the above-mentioned routers have been used as basic components in many of the recent works [12,27,31].

3. Main idea

3.1 Architecture

One of the characteristics of photonic communications is that buffers cannot be implemented for them [11]. Hence, unlike traditional chips that use packet switching methods, Circuit-Switching is used in photonic interconnections [20]. Different solutions have been proposed for implementing this method in photonic networks [3,21-23]. For instance, one of the strategies is using photonic signals with different wavelengths for transmitting data, in which each packet uses its path based on the signal's wavelength. One of the advantages of this structure is the ability of sending different data simultaneously by using different frequencies; However, one of the drawbacks in this structure can be the high cost and power dissipation of having different laser sources [24].

Another structure for controlling photonic communications is making use of electric control circuits, in which, unlike the previous structure, an electrical circuit is used as an arbitrator [3]. The disadvantage of this structure compared to the previous one is using electric controllers, that can increase power dissipation [7] . However, by considering the disadvantages of the previous structure, this structure has an admissible performance. This optical-electrical structure is named "Hybrid"..

3.2 Photonic Networks-on-Chip Elements

The type of photonic NoC considered in this paper is Hybrid which is composed of two parts: electrical and photonic.

3.1.1 Electrical Part

The electrical part is composed of wired communications and an electrical router. This router acts both as a controller and the arbitrator of the photonic network, and its structure is explained in [13].

3.1.2 Photonic Part

The photonic layer of a Hybrid network consists of waveguides, Laser-Detectors, Modulators and Micro Ring Resonators (MRR). Waveguides carry photonic messages. Modulators are devices that convert electrical signal to optical. Detectors are used at the end of an optical communication link and convert optical signal back to electrical. MRRs are used for deciding between continuing or changing data-paths on waveguides. Based on MRR physical characteristics, it can transfer photonic waves with specific resonance frequencies from one wave to another one. Of course, the MRR must be in "on" state in order to be able to transmit the signal. The on/off operation of the MRR is done by applying a voltage to the p area creating a channel between p and n layers (Fig. 1).[7] It should be noted that this functionality is used for controlling On-Off-Key (OOK) MRRs and thus for other kinds of MRRs such as Differential-Phase-Shift-Keyed (DPSK) MRRs, phase variation is used [25].

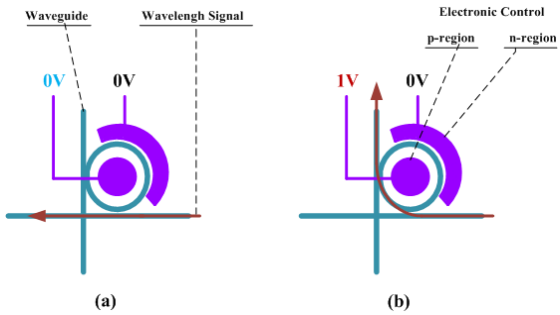

Fig 1 MRR physical attribute in two different states (a) "off-state", (b) "on-state"

3.2 Photonic Switching Element:

PSEs are the basic elements in PNoCs and are used in photonic routers. A PSE is composed of one MRR and two waveguides. Also, it has two different types (as shown in Fig. 2): parallel and cross.[15] The difference between the two types is the waveguide positioning. If

MRR is “on”, the signal will change its path and it will be forwarded to the “drop port”, otherwise the signal will continue its path and will be forwarded to the “through port”.

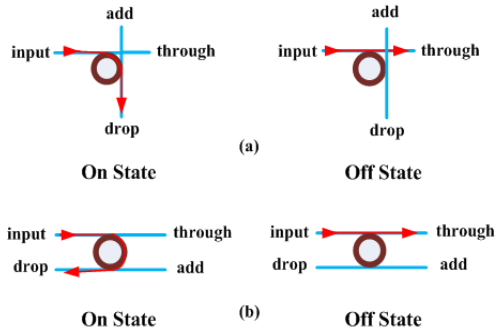

Figure 2. parallel and cross PSEs (a) cross PSE, (b) parallel PSE

Moreover, design factors can affect the functionality of PNoCs, which include: waveguide crossing and waveguide bend. Bending is formed when there is a bend in the waveguide, and cross is the intersection of two orthogonal waveguides. these two factors are the design elements of photonic routers and directly affect insertion loss in on-chip photonic communications. However, among design factors, waveguide crossing is of more concern [12,27].

3.3 Topology and Routing algorithm

In this paper we have used Mesh topology due to its simplicity and regularity. Its structure is shown in Fig. 3. In this topology, routers with 5 input and output ports are required. For simplicity, 4-port routers with Inject and Eject gateways have been used instead, as shown in Fig. 3[8][12]. As it can be seen in Fig. 4[12], the Inject and Eject gateways have been used instead of local ports connected to processing cores and therefore, they have resolved the router’s need for a fifth I/O port.

In addition, we have used XY routing algorithm, which is a deadlock-free DOR algorithm. Due to its simple implementation and deadlock-free, this algorithm is an appropriate choice. Therefore, the proposed router is designed in a way that can be used without the occurrence of blocking and with the minimum cost and highest performance, when XY routing algorithm is applied.

3.4 Our Design Approach

In this paper we have proposed a loss-aware router design approach which can lead to the design of a photonic router with a significant decrement in hardware redundancy and insertion loss. Such router can be implemented in networks with a higher bandwidth density and larger scales compare to fully-connected routers. This router specifically is designed for XY routing algorithm and can be exploited in Mesh and Torus topologies.

In addition, we have compared our proposed router with three other routers. The first one is named Original (Fig. 5a), consisting of 8 MRRs, 4 waveguides and 10 waveguide crossings [14]. The second router is called StraightPath(Fig. 5b), which is composed of 8 MRRs, 4 waveguides and 12 waveguide crossings [19]. The third one is named Symmetric (Fig. 5c), which has 8 MRRs, 4 waveguides and 8 waveguide crossings [19].

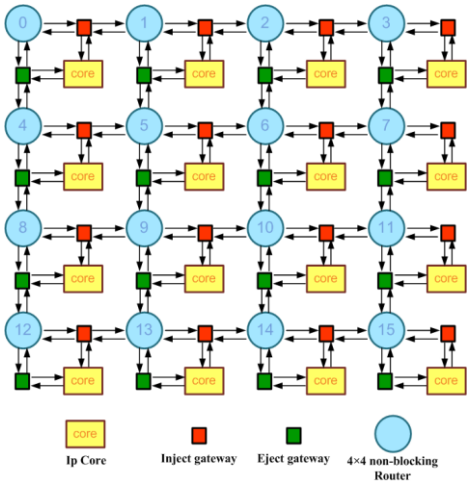

Fig 3.The structure of Mesh topology consisting of 4×4 non-blocking routers is shown by blue circles and Injection/Ejection gateways are shown by red/green rectangles

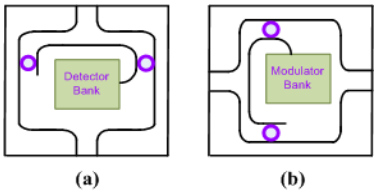

Fig 4. Eject/ Inject gateways. (a)Eject gateway, (b) Inject gateway

Since the previously proposed routers were Fully-Connected (Fig. 5), a large number of PSEs has been implemented in them in order to make connection between each input port with each output port. Also, the design complexity of Fully-Connected routers causes the number of crosses to increase. We have customized these routers for XY routing algorithm in order to provide a fair comparison. By customizing we mean that the extra components (i.e. extra PSEs) which are useless in XY routing are reduced. Even by customizing the routers (Fig. 6), no significant improvement will be achieved in insertion loss.

We have considered the below factors in our design approach:

- *Insertion Loss :* The frequent use of straight paths (i.e. east to west, south to north and

vice versa) in DOR algorithms has led us to have a special attention to such paths in the proposed design approach in order to obtain a lower insertion loss compared to other routers, when having transmission on such paths. For this purpose, firstly, we have tried to reduce the presence of on-state PSEs in such paths. Secondly, we try reducing crosses on such paths as much as possible.

- *Die Area:* Since it is not necessary in DOR algorithms to have connection between every port, we try to use less PSEs in the routers as much as possible.
- *Power Dissipations*: Since power consumption in photonic networks is affected by three elements, i.e. modulators, detectors and "on-state" PSEs [27, 31] and among these factors only PSEs are design-dependent, we have tried to reduce power consumption in such networks by decrementing the number of "on-state" PSEs on transmission paths. To achieve this goal, we avoid the situation in which "on-state" PSEs can exist on important paths (i.e. straight paths).

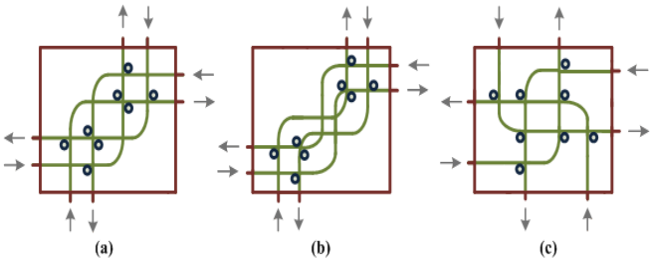

Fig 5. (a). Original Router, (b). StraightPath Router, (c). Symmetric Router

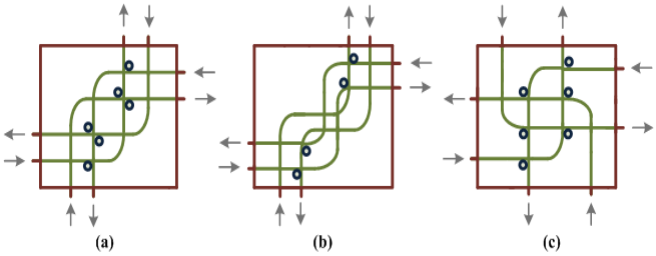

Fig 6. XY Routing-Customized Routers: (a). Original Router, (b). StraightPath Router, (c). Symmetric Router

According to the mentioned factors, our proposed approach is based on minimizing the number of "on-state" PSEs on direct paths and also covering all paths required by DOR algorithm by using the least number of PSEs and crosses.

Based on our design approach we have proposed a Non-blocking router (Fig. 7), particularly for supporting XY routing algorithm, The proposed router consists of 4 waveguides and 4 PSEs (2 parallel PSEs and 2 cross PSEs). Regarding the proposed approach, the number of PSEs is reduced compared to other proposed routers. Furthermore, the number of waveguide cross points in this router is 4. However, this router is designed in a way that all PSEs are in "off-state" when data is transmitted through a straight path and only 2 crosses exist along straight path. Since it does not require connection between every I/O port, the number of PSEs and crosses has reduced. This can in turn reduce the chip's hardware and area overhead.

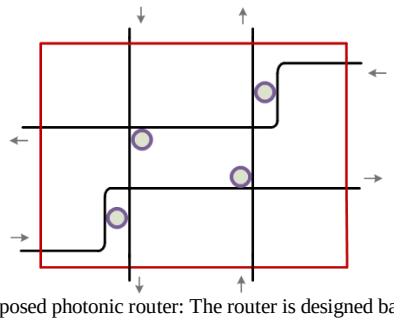
Fig 7. Proposed photonic router: The router is designed based on the proposed approach and works exclusively with XY routing algorithm

4. Experimental Results

In this section we will compare our proposed router with three other paradigms by means of PhoenixSim simulator [27] which will be explained in the rest of the paper. The simulation is done with regards to characteristics such as insertion loss and power dissipation. Also, photonic networks have been simulated by applying different traffic patterns and various network sizes. The main goal of this simulation is to assess the level of improvement in functionality in the proposed router when compared to other routers and thus to represent the improvement of PNoC characteristics by altering the design viewpoint.

4.1 Simulation environment

In this paper we have used PhoenixSim which is developed in Omnet++ environment [30] in order to evaluate the functionality of photonic Networks-on-Chip [27]. This simulator makes it possible to assess different scenarios with different network component configurations that can lead to a better analysis of PNoCs. However, the primary value of some of the physical components of the simulator must be set and initialized before running. We have set these valued based on [12] in which the fabrication results of the components have been proposed. For instance, the values of insertion loss and power dissipation for the basic PNoC components have been mentioned in Tables I and II.

In the simulation process, the die area has been 2cm × 2cm. Also, the network size varies from 4 to 256 nodes. Other important simulation configurations can be seen in Table III.

TABLE I. OPTICAL DEVICE INSERTION LOSS PARAMETERS

Parameter	Value
Propagation loss (silicon)	1.7 dB/cm
Waveguide crossing	0.16 dB
Waveguide bend	0.005 dB/90°
Drop into a ring	0.6 dB
Pass by a ring	0.05

TABLE II. OPTICAL DEVICE ENERGY PARAMETERS

Parameter	Value
Modulators (dynamic energy)	85 fJ/bit
Modulators (static energy)	30μW
Photo detectors	50 fJ/bit
PSEs (dynamic energy)	375 fJ/bit
PSEs (static energy)	400μW
Thermal ring tuning	100μW/ring

TABLE III. SIMULATION CONFIGURATION

Simulation Parameter	*Value*
I/O Bit Rate	2.5 Gb/s
Electronic Channel Width	32 bits
Message Size	1024 bits
Router Buffer Size	64
Processor Concentration	1
Max Packet Size	32 bits
Laser Power	10 dbm

4.2 Insertion loss

One of the analyzed parameters in this paper is insertion loss, which has been measured for different routers and different Mesh networks sizes, ranging from 2×2 to 16×16. The simulation is based on the primary data, which are resulted by physical experiments and listed in Table I. This measurement has been done under different traffic patterns including: All-to-All, Random and Tornado. The average value of insertion loss, when using the mentioned traffic patterns, has been depicted in Fig. 8 which, showing 52.65%, 48.34% and 39.77% improvements in comparison to Original, StraightPath and Symmetric routers under All-to-All traffic pattern, respectively. It is worth noting that since under all-to-all traffic pattern, signals are transmitted via all paths, maximum insertion loss will also be computed.

In order to evaluate insertion loss, firstly, we have Fully-Connected routers with different sizes and we have computed the loss value for each of them. Afterwards, as mentioned in the previous section, we customize the routers for XY routing algorithm and repeat the simulation. Indeed, since the number of waveguides and crosses cannot be changed, we have only removed the PSEs that were not required in XY algorithm. Simulation results of Fully-Connected and XY-customized routers in a 256-node network, and under all-to-all traffic pattern are displayed in Table IV. As can be seen, no significant improvement has been obtained in insertion loss between these two groups. This infers that it is necessary to change router design approach in order to achieve an efficient router, both for the specific topology and routing algorithm.

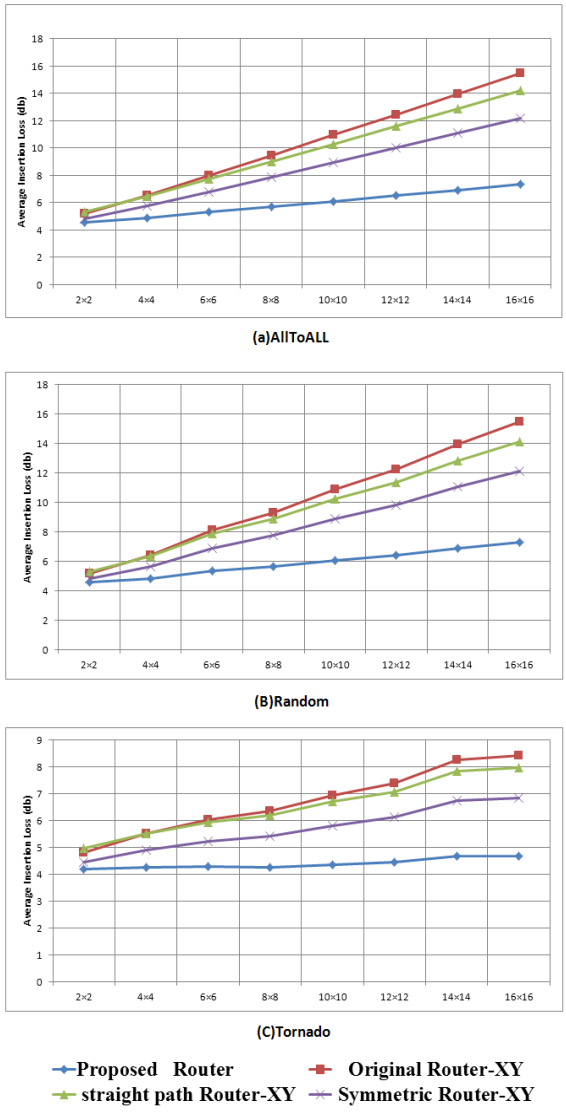

Fig 8. Average insertion loss results in various network dimensions with different traffic patterns

TABLE IV. AVERAGE INSERTION LOSS OF FULLY CONNECTED ROUTERS COMPARED WITH XY-CUSTOMISED ROUTERS IN 16×16 NETWORK SIZE

	Fully-Connected Router	XY_customized Router
Original	15.57db	15.48db
StraightPath	14.28db	14.18db
Symmetric	12.26db	12.17db

As it can be seen in Fig. 9, when examining insertion loss for router components, the most important components in loss analysis are crossing loss, drop into a ring(which denotes the insertion loss of "on-state" PSEs) and propagation loss, when the network size is 16×16 and All-to-All traffic pattern is used. As mentioned in section III, in XY routing algorithm, improvement in insertion loss depends on the number of crosses through straight paths. So, the proposed router with 2 crosses in these paths has achieved just 4.67 % Crossing loss improvement in comparison with Symmetric router due to having the same number of crosses on straight paths. But, it shows 51.2% and 66.67% improvement when compared to Original and StraightPath routers, because of having 3 and 6 crosses on their straight paths, respectively.

Also, since there is no need for "on-states" PSE in direct paths, the value of drop into a ring loss in the proposed router is the same as the StraightPath router and it is just 2 db, which shows an improvement of 69.76 % in comparison to the other two routers.

4.3 Power Budget and Network Throughput

One of the important factors when designing photonic NoC routers is the high bandwidth of such networks which its effective use can lead to improvements in throughput. One of the methods used in order to increase bandwidth performance in PNoC is Wavelength-Division-Multiplexing (WDM), which enables the transmission of multiple independent signals with different frequencies through only one waveguide [3,26]. It should be noted that as the number of parallel waves increases, the input power will be divided between the waves. Thus, the number of parallel photonic waves must not exceed a specific amount; otherwise, due to the constraints present in detector sensitivity the correct detection of photonic waves can become difficult.

Due to the constant value of detector sensitivity we can increment the number of parallel signals transmitted through the waveguide by increasing the input power. It should be noted that increasing the power above a specific level can lead to the exponential growth of insertion loss instead of linear; thus it can make the network inefficient. This value is constant according to the manufacturing technology and is named "Power Threshold". Therefore, the interval range of network's input power is bounded to the detector sensitivity and Power- Threshold and cannot exceed these limits.

According to what mentioned above, in order to determine the maximum possible network insertion loss and the maximum number of parallel wavelengths in case of using networks consisting of multiple wavelengths links, we use the power budget parameter, which equals the difference between the input power and the minimum power, sensible by the detector measured in Decibels [9,12].

$$P\_S \geq IL_{MAX} + 10log_{10}\, n \quad (1)$$

In equation (1), P is the total power, S is the detector sensitivity, IL_{Max} represents the maximum insertion loss and n denotes the maximum number of available parallel wavelengths in the network.

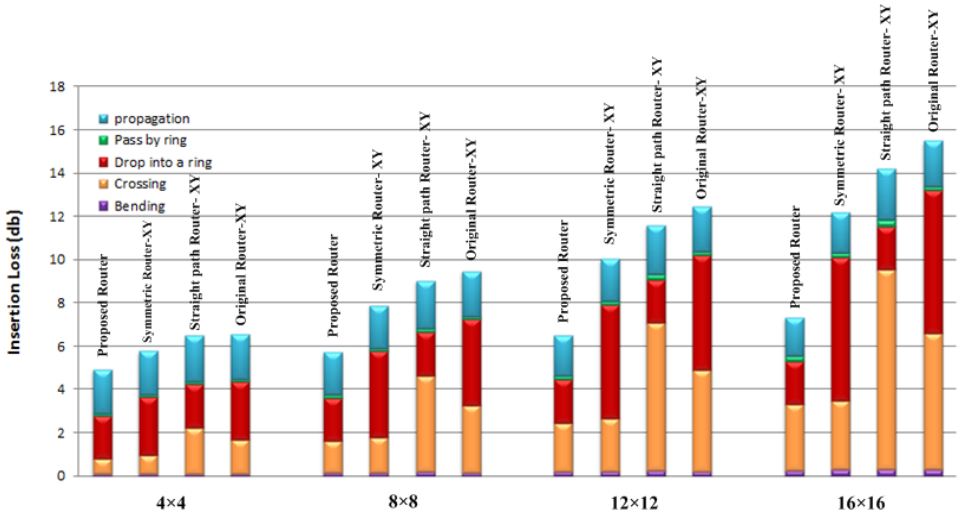

Fig 9. Insertion loss of effective components in evaluated photonic routers

If we consider the input power 10 db, the detector sensitivity equal to -20 db and obtain the maximum insertion loss by simulation, by using the all-to-all traffic pattern (shown in Fig. 10) and by means of equation (1), the maximum number of PNoC wavelengths can be computed for different network sizes and different routers. Additionally, based on the results, maximum admissible network sizes can be observed in Fig. 11. Hence, the Original and StraightPath routers can be employed in Mesh networks with up to 100 nodes, whereas the Symmetric router can be used in a network with 144 nodes. Not only the proposed router can be used in a network with 256 nodes, but it also supports 18 parallel wavelengths in this network size. Also, the proposed router can support 34 and 46 parallel wavelengths in networks with 144 and 100 nodes, respectively.

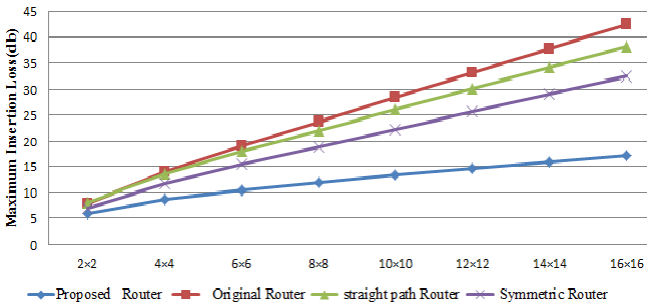

Fig 10. Maximum insertion loss in various network sizes with All-to-All traffic pattern

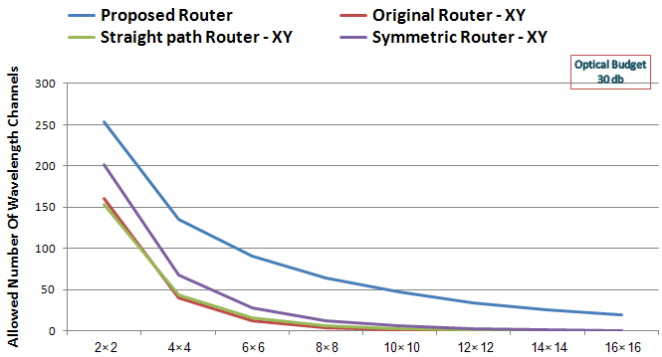

Fig 11. Number of available wavelengths in various network sizes

4.4 Power Dissipation

The other parameter, analyzed in this paper is the dissipated power which is composed of electrical power which has a higher share and optical power in PNoCs [12]. The simulator used, PhoenixSim, makes use of ORION 2.0 library in order to compute the electrical power consumption [28] in which the physical power parameters are considered based on the entries of Table II, and the fabrication technology is considered 32 nm. The value of electrical power is the same for all 4 routers. Thus, it can be seen that no significant improvement has been occurred in the total power. However, the photonic power of the proposed router demonstrates 18.75%, 4.07% and 14.78% improvement when compared to the Original, StraightPath and Symmetric routers, respectively.

As illustrated in section III, and is depicted in Fig. 12, the difference between routers relies on "on-state" PSEs. Based on the importance of straight paths in XY routing Algorithm, "on-state" PSEs in straight paths could determine the difference amount among them [29]. The proposed router does not have any "on-state" PSEs On straight paths so its power dissipation is approximately similar to StraightPath router. However, due to the existence of an "on-state" PSE in straight paths of Original and Symmetric routers, 18.75% and 14.78% improvements are achieve by proposed router, respectively.

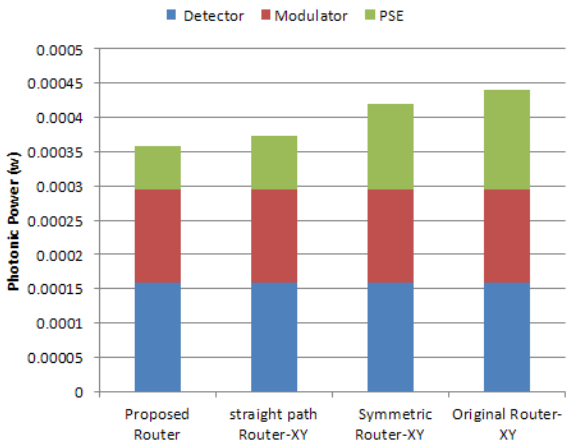

Fig 12. Power dissipation results of photonic component for a 256-node network under All-to-All traffic pattern

5. Conclusions

It can be observed that by considering the topology and the routing algorithm in the design of a photonic router, a significant improvement can be achieved in insertion loss. As mentioned before, the low number of PSEs and crosses in the proposed router can be considered as two of the important factors affecting loss value. One of the other advantages of our approach is that it does not require "on-state" PSEs in straight paths, which has led to the reduction of maximum network insertion loss and has enabled the possibility of implementing PNoCs with larger sizes, or WDMs with more parallel wavelengths. Additionally, our proposal has led to the reduction of die area, and also introduced a slight improvement in power dissipation, which is due to the improvement of photonic power.

As future works, the design of different routers can be explored both for a variety of topologies beyond the Mesh and Torus topologies and also for a wider range of routing algorithms.

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