An Efficient Single Impedance Network Three Level Z-Source Neutral Point Clamped Inverter

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Abstract

A multilevel inverter can eliminate the need for the step-up transformer and reduce the harmonics produced by the inverter. Although the multilevel inverter structure was initially introduced as a means of reducing the output waveform harmonic content, it was found that the dc bus voltage could be increased beyond the voltage rating of an individual power device by the use of a voltage clamping network consisting of diodes. By using voltage clamping techniques, the system KV rating can be extended beyond limits of an individual device. This paper presents Impedance (Z) Source Neutral Point Clamped (NPC) three level inverter with reduced number of impedance source networks and clamping diodes for non-linear loads. Earlier for a three level NPC inverter two separate impedance networks were used. But to reduce the circuit complexity without compromising with output requirement; only one impedance network is used and to substantiate this, the simulation of proposed circuit is carried out using MATLAB/Simulink for a 48 V input supply. A prototype is developed for an input voltage of 26V and the experimental results for the same are presented in this paper.

Keywords: Z-Source, NPC inverter; Two-level inverter, Three level inverter, Non-linear loads

1. Introduction

The Z-source NPC is a kind of single stage multilevel inverter which has the ability of voltage boost [1], But the boost capability is relatively low when they are subject to the renewable sources.

The Z-source converter employs an impedance circuit which connects the power source to the converter circuit thus providing unique features that cannot be obtained in the conventional Voltage Source Inverter (VSI) and Current Source Inverter (CSI); where a capacitor and inductor are used respectively [9]. The Z-source inverter overcomes limitations of the traditional VSI and CSI. The conventional voltage source inverter (VSI) can only produce an output voltage that is lower than the supply voltage of the battery. The maximum output voltage obtainable is limited by the dc bus voltage. For battery supplied electric vehicles, the dc-dc boosted inverter has the useful feature to either buck or boost the batteries voltage to a desired output voltage.

Multilevel converters have many advantages which are the capacity to generate a very good quality of waveforms, the reduced switching frequency, the low energy loss and the low effort on power devices [2, 6]. Three-level neutral-point-clamped (NPC) inverters, having many inherent advantages are commonly used as the preferred topology for medium voltage ac drives. These inverters have recently been explored for other low-voltage applications including grid-interfacing power converters to improve the power quality [5, 6 & 7].

The semiconductors of the Z-Source inverter experience additional stress during boost operation with respect to conventional VSI or the DC-DC boosted VSI. This stress has to be taken into consideration for the Z-Source inverters design. By the use of a Z-Source neutral-point-clamped (NPC) inverter, proposed in [4], and [5], these effects can be lowered. With respect to the two-level topology voltage stress across the switches are cut in half. Furthermore the quality of the output waveform can be improved through the introduction of a third voltage level.

Z-source NPC three level inverter with single Z-source network is more efficient compared to conventional scheme where the number of impedance networks requirement increases with increase in the number of input level. The present paper aims at overcoming this drawback, where-in irrespective of number of levels in MLI, a single impedance network along with clamping capacitors is used. Therefore the inductors in circuit are reduced enabling compact and efficient design.

2. Z-Source Three Level Inverter

The conventional Z-source NPC three level inverter is shown in Fig.1. This circuit uses two impedance networks as shown in Fig.1. The Z-source network can boost input DC voltage. Consequently two boost factors can be defined for Z-source NPC inverter as:

$$V_{iU} = B_U V_{oU} = \frac{V_{oU}}{1-2(T_{SCOU}+T_{SCB})/T} \quad (1)$$

$$V_{iL} = B_L V_{oL} = \frac{V_{oL}}{1-2(T_{SCOL}+T_{SCB})/T} \quad (2)$$

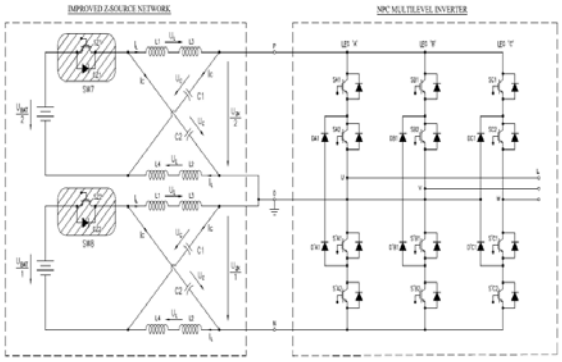

Fig.1 Conventional Three Level NPC Inverter

Where V_{oU}, Vo_L are DC input voltages and Vi_U, Vi_L are DC link voltages. T_{SCOU}, T_{SCOL} and T_{SCB} are the shoot-through time intervals of only upper z-source network output, only lower output and both outputs, respectively. For low output THD, boost factors should be determined such that voltage of both DC links of inverter would be the same. In NPC inverter, if both DC links are the same, equal powers are extracted from both DC links.

The proposed circuit to obtain same output levels same as in circuit in Fig.1 is shown in Fig.2. It uses only one impedance network. The operation is similar to circuit in Fig.1. The DC link voltages are given by

$$V_{iU} = V_C - V_{oL} \quad (3)$$

$$V_{iL} = V_C - V_{oU} \quad (4)$$

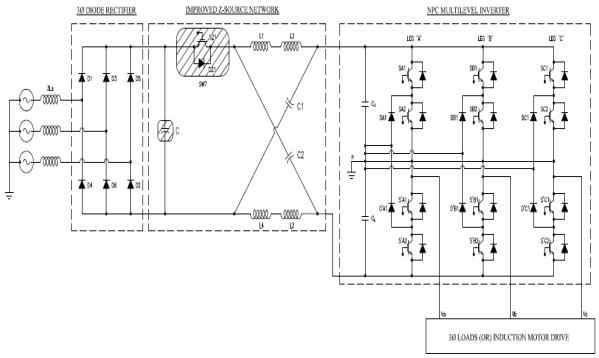

Fig.2 Proposed Z-source Three Level NPC inverter

3. Simulation Results

The simulation is carried out using MATLAB/Simulink. The simulation circuit is shown in Fig.3. Input is 48V DC which is shown in Fig.4.

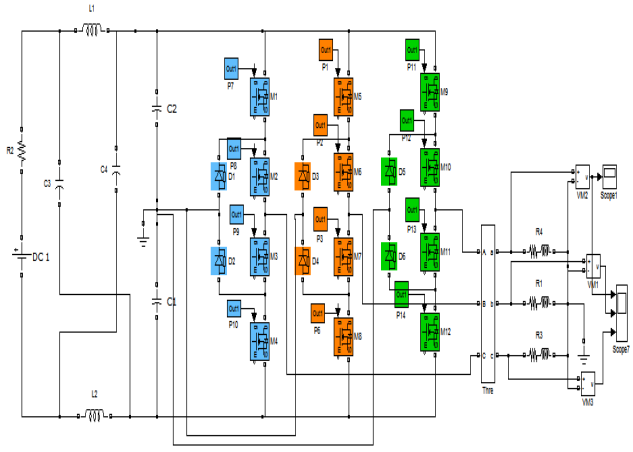

Fig.3. Simulation circuit diagram of prosed Z-source Three Level NPC inverter

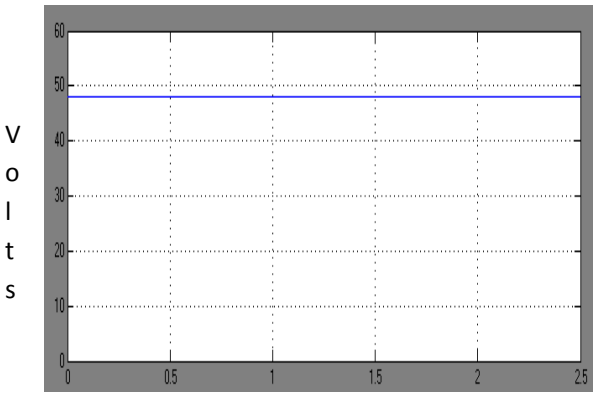

Fig.4 DC input volatge T(ms)

The gate pulses for MOSFET's in first leg M1 – M4 are shown in Fig.5. The phase output voltages in Leg 1 are shown in Fig.6. The proposed inverter Phase volatges in all three legs are shown in Fig.7. The line voltages of proposed three phase three level Z-source inverter are shown in Fig.8. Three phase currents are shown in Fig.9. The FFT analysis is done to find the Total Harmonic Distortion (THD) and the FFT results are shown in Fig.10

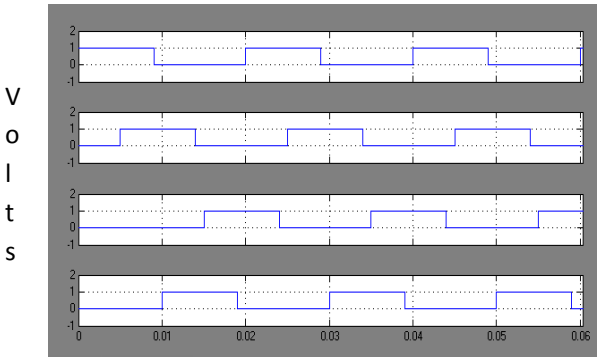

Fig.5 MOSFET Gate Pulses (I- Phase) T(ms)

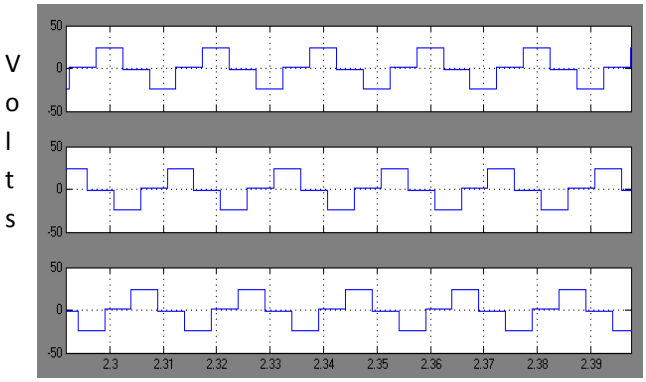

Fig.6 Phase Voltages in Leg 1 (I-Phase) T(ms)

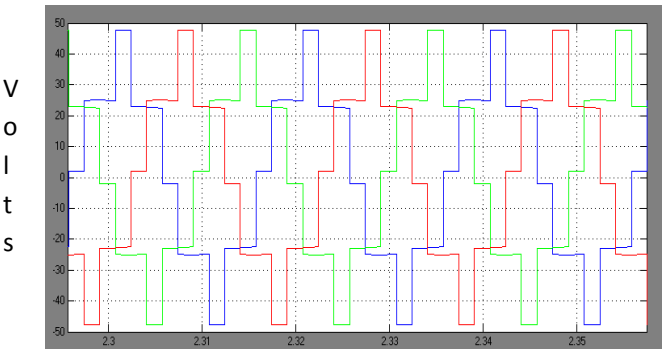

Fig.7 Per Phase Voltage in Three Legs T(ms)

As observed from Fig.7, three levels 110 V, 48 V and Zero voltages are obtained.From this it is concluded that a single impedance network is sufficient to obtain the required levels.

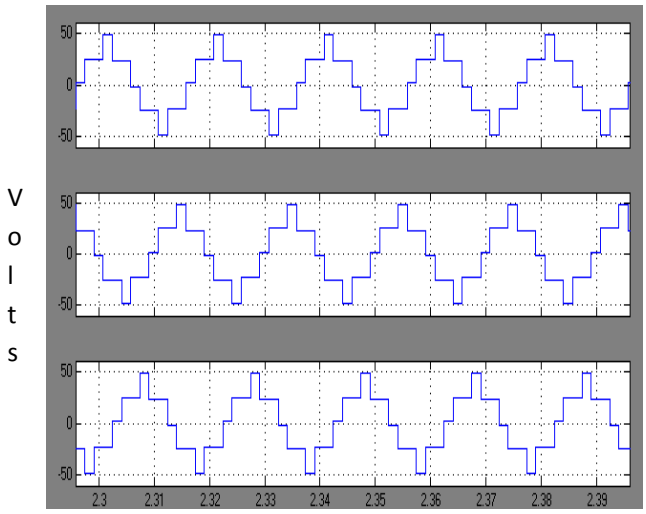

Fig.8 Line Voltages of proposed circuit T(ms)

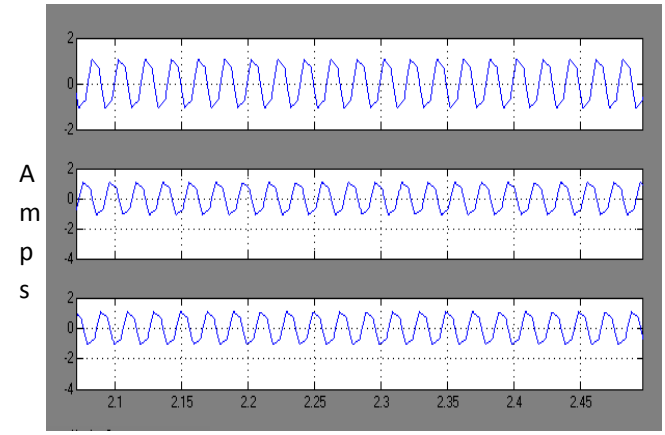

Fig.9 Three Phase Output Currents T(ms)

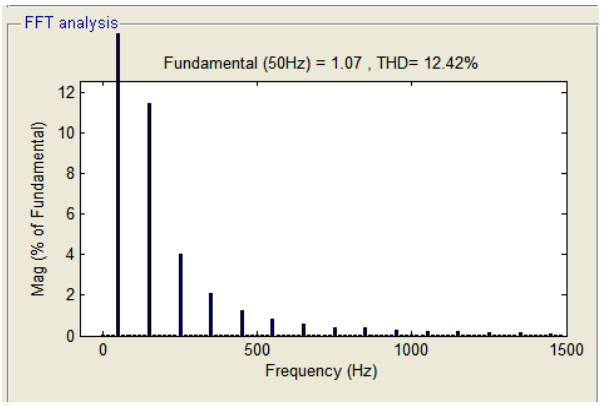

Fig.10 FFT Analysis Results.

The THD is 12.42%.

4. Experimental Results

The experimental set up is shown in Fig.11. The input voltage is 26V, which is shown in Fig. 12. The output of driver circuit is shown in Fig.13. The complementary switching pulses for upper and lower switches are shown in Fig.14. The inverter output voltage is shown in Fig.15

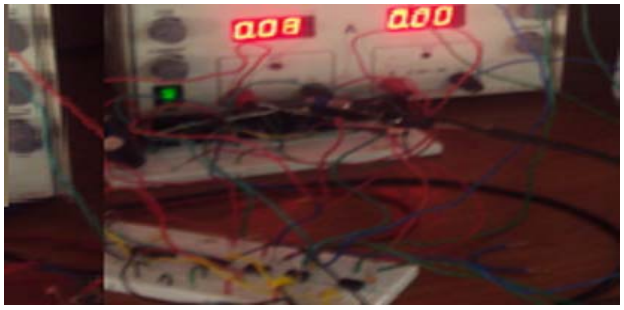

Fig.11 Experimental Set up

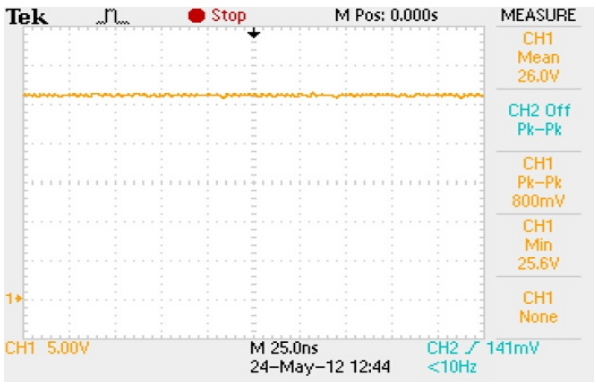

Fig.12 Input voltage

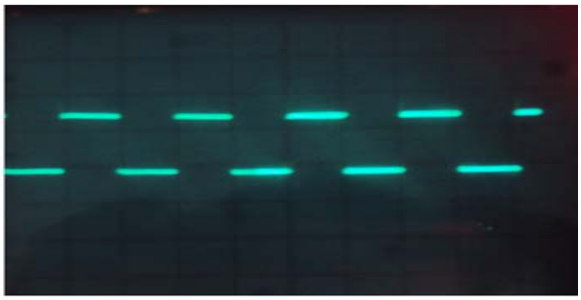

Fig.13 Output of Driver circuit.

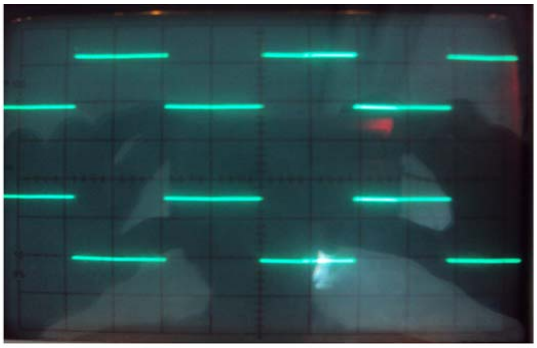

Fig.14 MOSFET Switching pulses

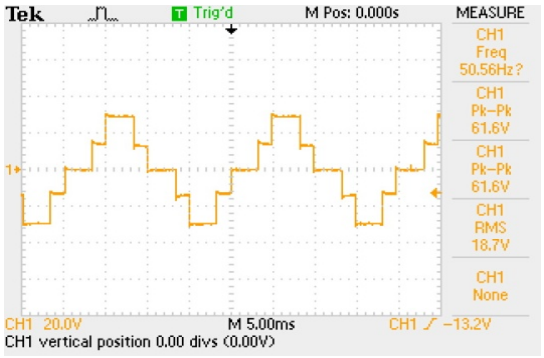

Fig.15 Inverter Output voltage

5. Conclusion

A novel Z-source Three level NPC with single impedance source network is proposed. As observed from the simulation results from Fig.7 to Fig.9, it is concluded that the proposed circuit can replace the conventional Z-source NPC in verter where two impedance source networks are used. Since the number of inductors in the proposed circuit are reduced, EMI is less and the circuit is

simple and economical and more efficienct compared to the conventional circuit. The THD of proposed converter is 1 2.42%. The simulation results are experimentally validated.This work can be further extended to higher levels to minimize the THD can be further reduced by increasing the number of levels.

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