Design of a Novel Voltage Regulator Module (VRM) with Fast Transient Response

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Abstract

In this paper, a new circuit of power supply for microprocessors, named as switched-inductor multiphase voltage regulator module (VRM), is presented and designed. One of the main requirements of VRMs for today's microprocessors is fast transient response. The other issues associated with conventional VRMs are small duty ratio, large ripple and low efficiency. A solution to the limitations of these VRMs is presented in the form of a new VRM topology which is obtained from the multiphase interleaving VRM by the addition of a capacitor and introduction of a second inductor in each phase. The proposed VRM has the advantage of extending the duty ratio, decreasing the peak-to-peak ripple and a very fast load transient response. Both theoretical and simulation results shows that the performance of the proposed VRM is better than the conventional VRMs. The proposed VRM operates with double duty ratio and has fast transient response, small ripple and reduced voltage stress on switches, which improves efficiency.

Keywords: VRM, multiphase, transient response, voltage stress

1. Introduction

Nowadays, microprocessors are becoming very powerful and their power needs are increasing with the passage of time. This advancement in processor technology imposes great challenges in designing power supplies for these devices. Modern microprocessors require power supplies with high output current, low output voltage, high efficiency and fast transient response. In order to meet the present power requirements of microprocessors, a special dc-dc converter, called the voltage regulator module (VRM) is used. Earlier, these VRMs were supplied from a 5-volt silver box source. Nowadays, the VRM for microprocessor is supplied from a 12-volt input of silver box on mother board [1, 2].

The simplest form of a VRM is a simple buck converter or synchronous rectifier buck converter. For modern microprocessors, the drawbacks of these topologies are clear as they use large inductors to reduce inductor current ripple. These large inductors decrease the output current slew rate (di/dt) and results in slow transient response. Due to this reason, most of today's VRMs use multiphase interleaving buck converters or multiphase interleaving synchronous rectifier buck converters. These multiphase VRMs produce current ripple cancellation effect, which allows the use of small filter inductors and results in improved transient response. It is clear from above discussion, that the transient response of a VRM is inversely proportional to the filter inductance. If a VRM uses small filter inductance, then its transient response is fast. However, small filter inductance increases the ripples in output current and voltage. Thus designing a VRM with fast transient response and small ripple is a serious technical challenge [3,10].

Most of today's VRMs operate at an input voltage of 12 volts and output voltages around 1 volt. Thus, the requirement for VRMs is a high step-down voltage conversion. Consequently, they operate with very small duty ratios. This increases the conduction losses of the diode of buck converter and cause asymmetry in step-up and step-down load transient response. Due to high step-down conversion, the rate of increase of output current is higher as compared to its rate of decrease. This results in fast step-up load transient response as compared to step-down load transient response. The high voltage stresses (off state voltage of switch) of switching devices are also major concerns in high step-down converters as high current and voltage stress of switch directly increases the switching losses and decreases the efficiency [1,6]. In summary, today's VRMs suffer from slow transient response, high voltage stress of switching devices, small duty ratio and low efficiency.

A lot of research has been done on VRM and a number of methods have been proposed to improve the transient response and extend the duty ratio of a VRM.

A method in which hysteretic control technique is used in the closed loop of VRM is presented [4]. Unlike a PWM control in which the switching frequency is fixed,

hysteretic control works on variable switching frequency. This method is good as it provides fast transient response. However, this method has the problems of variable switching frequency and non-zero steady-state error.

A multiphase interleaving technique has also been used to obtain fast transient response [3]. A multiphase buck converter is used to reduce the amount of inductance required. In this technique, there is a ripple cancellation effect and the output current has small ripple. This relaxes the requirements of the output and input filters. As small filter inductance is needed, transient response is fast. This technique improves the transient response, but the performance of this VRM is not satisfactory due to high switching loss. In addition, there is a problem of phase current sharing.

Another technique that involves the use of coupled inductors is used to improve the transient response [5]. In this technique, the inductors of the two phases of a two-phase converter are magnetically coupled to each other. This helps in the reduction of phase current ripples. Moreover, the converter uses small leakage inductance as the equivalent inductance in the transient state. Hence, the transient response is fast. Coupling helps in improving the transient however, the performance depends on the extent of coupling, as it is very difficult to perfectly couple inductors. Moreover, there is leakage inductance, which increase losses and decrease efficiency.

A technique in which coupled inductors are used to increase the duty ratio is presented [7]. There are two additional coupled winding in each phase with a turn ratio of n. The duty ratio is extended by increasing the number of turns of coupled windings. This is a good method for extending the duty ratio, but there is a leakage inductance that increases losses.

A two-stage approach has been presented to extend the duty ratio [8]. In this approach, the voltage conversion is done in two stages to extend the duty ratio. A 12 volt input is converted to 1 volt output in two stages. The first stage conversion is from 12 volts to 5 volts at low switching frequency, and the second stage conversion is from 5 volts to 1 volt at high switching frequency. This approach extends the duty ratio. However, it is more complicated as compared to the single-stage approach.

2. Proposed Switched-inductor VRM

Research is ongoing on VRM and several forms of VRM are available nowadays. Various people have presented a number of methods discussed earlier but they fail to solve all the issues related to a VRM. A solution to the limitations of today's VRM is presented here in the form of a new proposed VRM topology named switched-inductor multiphase VRM. This proposed VRM is a modified form of a two-phase synchronous rectifier VRM with an additional capacitor at its input section and introduction of a second inductor in each phase, which can be switched in and out of circuit. The circuit diagram of this VRM is shown in Fig. 1.

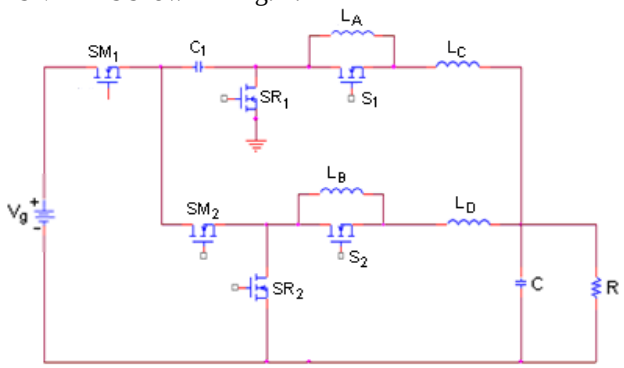

Fig. 1: Switched-Inductor Multiphase VRM

There are total six switches in the proposed VRM. The switch SM_1 is the main switch of phase#1 and switch SR_1 is its synchronous rectifier. Similarly, switch SM_2 is the main switch of phase#2 and switch SR_2 is its synchronous rectifier. Switches S_1 and S_2 are the transient switches and are off in normal condition and operate only in load the transient condition to short the inductors connected across them. Switches SM_1 and SR_1 operate synchronously, that is, when SM_1 is on, SR_1 is off and vice versa. Similarly switches SM_2 and SR_2 operate synchronously. In this VRM, each phase contain two separate inductors. Phase#1 contains inductor L_A and inductor L_C. Similarly, Phase#2 contains inductor L_B and inductor L_D. These inductors are such that:

$$L_A = L_B,\ L_C = L_D,\ Lc = 1/n\ .L_A\ ,\ L_D = 1/n\ L_B$$

$$L_A + L_C = L_1 \quad \& \quad L_B + L_D = L_2$$

$$Lc = (1/n+1).L_1,\ L_D = (1/n+1).\ L_2,\quad L_1 = L_2 = L$$

n is a variable and is taken to be equal to 3 (n =3). L_1 is the total inductance of phase#1 and L_2 is the total inductance of phase#2; both these inductances are equal.

2.1 Steady state analysis

In steady state, switches S_1 and S_2 are open and the two inductors in each phase are in series. L_A and L_C are in series and their equivalent inductance is L_1. Similarly, L_B and L_D are in series and their equivalent inductance is L_2. The circuit diagram of the proposed VRM in steady state is shown in Fig. 2.

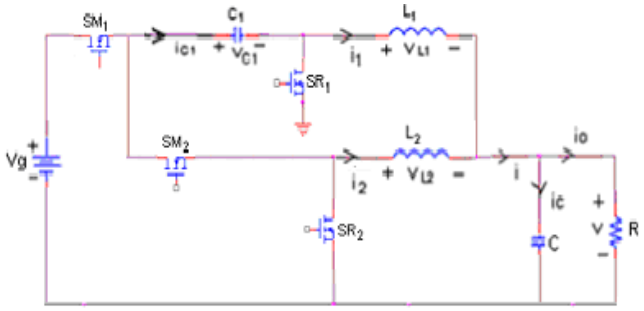

Fig. 2: Switched-Inductor VRM in Steady State

The switched-inductor multiphase VRM operates on fixed frequency (Fs) and thus on fixed switching period (Ts). There are four states of operation in one switching period.

In state I, switches SM_1 and SR_2 are on and switches SM_2 and SR_1 are off. The time for this state is from 0 to DTs. In this state the source supplies energy to load through capacitor C_1 and inductor L_1. Therefore Inductor L_1 and capacitor C_1 store energy; current i_1 through L_1 and voltage Vc_1 across C_1 rise linearly. Inductor L_2 also supplies energy to the load. Hence, inductor L_2 discharges and current i_2 through it decreases linearly. The output capacitor C also stores energy and output voltage increases linearly.

At the start of state II, switch SM_1 turns off and switch SR_2 is still on. Therefore, Switch SR_1 turns on and switch SM_2 is still off. The time for this state is from DTs to Ts/2. In this state, the input source voltage is disconnected from both phases and the load. Inductors L_1 and L_2 supplies energy to load and discharges. Currents i_1 and i_2 decrease linearly. Input capacitor C_1 neither charges nor discharges; current ic_1 through it is zero and voltage across it is constant. The output capacitor C discharges and output voltage decreases linearly.

At the start of state III, the switch SR_2 turns off and switch SR_1 is still on. Therefore, Switch SM_2 turns on and switch SM_1 is still off. The time for this state is from Ts/2 to Ts/2+DTs. Inductor L_1 supplies energy to load and discharges. Current i_1 through L_1 falls linearly. Input capacitor C_1 discharges in this state and supplies energy to load through inductor L_2. Hence, voltage across C_1 falls linearly. Inductor L_2 stores energy and current i_2 through it rises linearly. The output capacitor also stores energy and output voltage increases linearly. State IV is the last state of the switching period and is similar to state II. The time for this state is from Ts/2 + DTs to Ts.

The output voltage of the proposed VRM, which is determined by the application of Kirchhoff's Current Law (KCL), Kirchhoff's Voltage Law (KVL) and inductor volt-second balance principle is given by:

$$V = \frac{DVg}{2} \quad (1)$$

The above equation shows that the output voltage (V) is equal half of the product of the duty cycle (D) and input voltage (Vg).

Again by the application of KVL, KCL and inductor-volt second balance principle, the voltage across the input capacitor C_1 is obtained which is same as the output voltage and is given by:

$$Vc_1 = \frac{DVg}{2} \quad (2)$$

Similarly for output current equation, the principle of capacitor charge balance is used and the output current (I) of proposed VRM is given by:

$$I = I_1 + I_2 = \frac{DVg}{2R} \quad (3)$$

Again by the application of capacitor charge balance principle the current though phase#1 (I_1) and the current through phase#2 (I_2) are given by:

$$I_1 = I_2 = \frac{I}{2} \quad (4)$$

The above equation shows that the phase currents are equal during the entire operation of VRM. Hence there is an automatic phase current balance and the proposed VRM does not need any additional current sensing and balancing circuit.As discussed earlier the current through inductor L_1 or phase#1 is increasing in state I and decreasing in the rest of switching period. The peak-to-peak ripple in the current through inductor L_1 is given by:

$$\Delta i_1 = \frac{Vg(1-D)DT_S}{4L_1} \quad (5)$$

Where L_1 is the inductance of phase#1 and Ts is the switching time period. Similarly, the current through inductor L_2 or phase#2 is increasing in state III and decreasing in the rest of switching period. The peak-to-peak ripple in the current through inductor L_2 is given by:

$$\Delta i_2 = \frac{Vg(1-D)DT_S}{4L_2} \quad (6)$$

Where L_2 is the total inductance of phase#2. The peak-to-peak ripple in output current is obtained by the addition of phase current ripples and is given by:

$$\Delta i = \frac{Vg(1-2D)DT_S}{4L} \quad (7)$$

Similarly the peak-to-peak ripple in voltage across the input capacitor C_1 is given by:

$$\Delta Vc_1 = \frac{I_1 DT_S}{2C_1} \quad (8)$$

I_1 is the average or dc value of current through phase#1. Finally the peak-to-peak ripple in the output voltage is estimated by the output current ripple and is given by:

$$\Delta V = \frac{Vg(1-2D)DT_S^2}{64LC} \quad (9)$$

There are total six switches in proposed VRM but the two switches S_1 and S_2 are used only in the transient condition and are off in steady state. When a switch turns on or off, there is a voltage drop across it called voltage stress of a switch, which will introduce losses and lowers the efficiency. The voltage stress of a switch is equal to the maximum voltage across it. By the application of inductor volt second balance principle the voltage stress of switch SM1 (V_{SM1}), voltage stress of switch SR1 (V_{SR1}), voltage stress of switch SM2 (V_{SM2}) and voltage stress of switch SR2 (V_{SR2}) are given below.

$$V_{SM1} = Vg - Vc_{1(min)} = Vg - (Vc_1 - 0.5\,\Delta v_{C1}) \quad (10)$$

$$V_{SR1} = V_{C1\,(min)} - Vg = (Vc_1 - 0.5\,\Delta v_{C1}) - Vg \quad (11)$$

$$V_{SM2} = Vg \quad (12)$$

$$V_{SR2} = - V_{C1\,(max)} = - \{Vc_1 + 0.5\,\Delta v_{C1}\} \quad (13)$$

Where, Vc_1 is the average voltage across input capacitor C_1.

2.2 Transient state analysis

When load current changes, the VRM goes through a load transient condition. This load transient affects the output voltage of the VRM. The slew rate of output current has a direct effect on the transient response of VRM. The circuit diagram of proposed VRM in load transient condition is shown in Fig. 3.

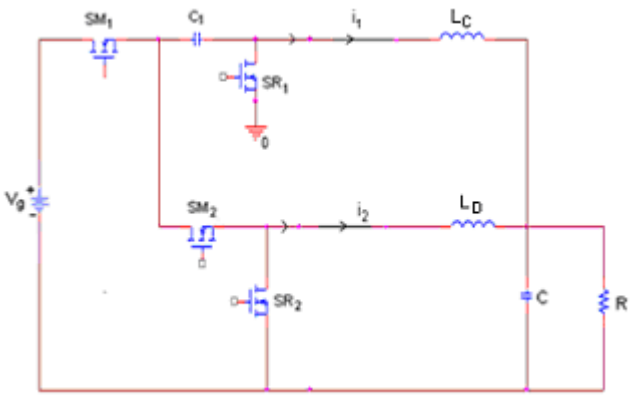

Fig. 3: Switched-Inductor VRM in load transient condition

Now, consider the load current decrease suddenly. This will cause the proposed VRM to go through a step-down load transient. During this condition the switches S_1 and S_2 in the proposed VRM turns on and shorts inductors L_A and L_B connected across them. Now, for a total decrease of ΔI in the output or inductor current, the time (T_{down}) taken by the output current to attain the required level is obtained by dividing the total change in output current by the output current slew rate, that is, di/dt [6]. The output current is equal to the sum of phase currents and its slew rate is equal to the sum of the slew rates of phase currents. The slew rates of the phase currents during a step-down load transient condition are determined by the voltages across the inductors L_1 and L_2 in state II or IV of VRM. The slew rate of the output current is equal to the sum of the slew rates of phase currents and is given by:

$$\frac{di}{dt} = \frac{di_1}{dt} + \frac{di_2}{dt} = -\left[\frac{V}{L_C} + \frac{V}{L_D}\right] \quad (14)$$

As already discussed that inductor L_C is equal to (1/n+1) L_1 and inductor L_D is equal to (1/n+1) L_2 and both inductors L_1 and L_2 are equal to L. Therefore, the time required by the proposed VRM to recover the voltage overshoot in a step-down load transient condition is given below.

$$T_{down} = -\frac{\Delta IL}{2(n+1)V} \quad (15)$$

Similarly, in a step-up load transient condition which is caused by a sudden increase in the output or load current, the time T_{up} required by the proposed VRM to recover the output voltage undershoot is given by:

$$T_{up} = \frac{1}{n+1}\left(\frac{\Delta IL}{V - V_{C1} - 2V}\right) \quad (16)$$

2.3 Control Loop

To regulate the output voltage of switched-inductor VRM a negative feedback is used in the closed loop. Various control loops of different converters have been studied and an idea about the control loop of switched-inductor VRM is developed according to its requirements. The circuit diagram of switched-inductor VRM along with its closed loop is shown in Fig. 4. There are total six switches in switched-inductor VRM. The PWM signal for each switch is generated from the control loop via negative feedback. The first element of the closed loop is sensor and is used to sense the output voltage and multiplies it with its gain H. The error amplifier is an operational amplifier, which subtracts the sensed output voltage from the reference voltage and obtains an error signal or error voltage Ve. An interleaved saw tooth generator is used which produces two saw tooth voltage signals also called the ramp signals with 180 degree phase shift. These ramp signals are shown in Fig. 5(a). There are two comparators that produce two PWM signals as shown in Fig. 5(b). D_1 is the duty ratio or PWM signal for switches SM_1 and SR_1 and D_2 is the duty ratio or PWM signal for switches SM_2 and SR_2. A comparator window comprised of two comparators (comparator#3 and comparator#4) is used to produce the PWM signals for switches S_1 and S_2 and operate these switches only in load transient condition. One input to both comparator#3 and comparator#4 is the error voltage Ve. Two reference voltage signals V_{High} and V_{Low} are applied at the remaining two terminals of both the comparators of window. The magnitude of voltage signal V_{High} is equal to the permissible increase in the error

voltage Ve or output voltage V. Similarly the magnitude of voltage signal V_{Low} is equal to the permissible decrease in the error voltage Ve or output voltage V. As long as the error signal Ve is within the window (less than V_{High} and greater than V_{Low}), the output of each comparator#3 and 4 is zero and switches S_1 and S_2 are off. When the error signal Ve increases above V_{High}, (step-down transient) or decreases below V_{Low} (step-up transient), the output of the comparator window is high and switches S_1 and S_2 turns on. This operation is described in Fig. 5(c).

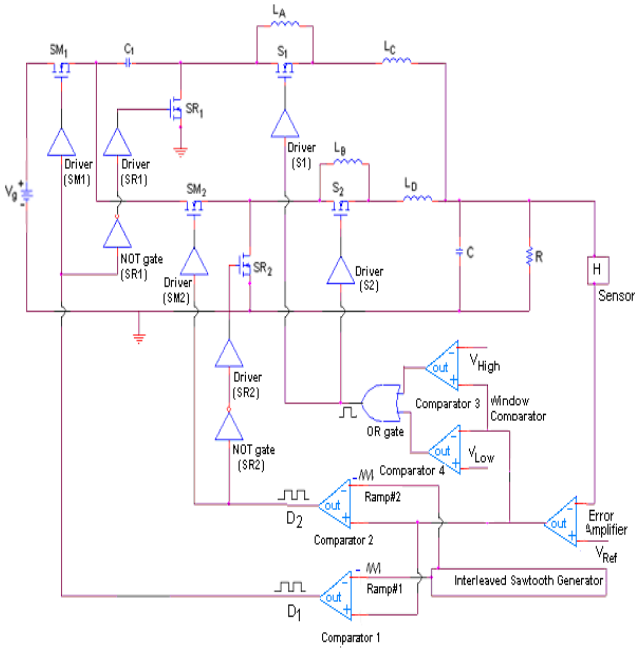

Fig. 4: Switched-Inductor VRM with closed loop

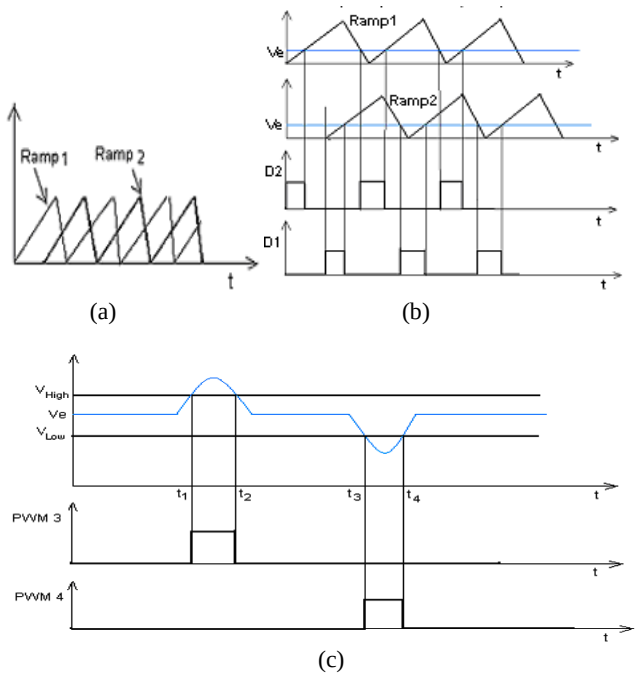

Fig. 5: Closed loop operation (a) interleaved ramp voltages (b) PWM in cmparator#1 and 2 (c) PWM in window comparator

2.3 Design and Simulations

The switched-inductor VRM is designed for suitable required specifications. Usually, the input voltage of a VRM is 12 volts. For the design of switched-inductor VRM, the input voltage source is also taken as 12 volts, output voltage is 1.8 volts and load is 0.1 ohms. The proposed VRM is operated at a frequency of 200 Khz (100 Khz/phase) and the maximum load current is taken as 36 amperes.

In order to verify the effectiveness of switched-inductor VRM, its theoretical and simulated results are obtained by using the following specifications:
Vg = 12V, V = 1.8V, R = 0.1 ohm, C = 15 uF
Fs = 100 Khz, $L_1 = L_2 = L = 7$ uH, $C_1 = 45$ uF,, $\Delta I = 13.4$ A

Theoretical Results: Using the specification and the equations of switched-inductor VMR, the following results are obtained.

D = 0.3, $Vc_1 = 6$ V, I = 18 A, I1 = I2 = 9 A , $\Delta i = 1.03$ A,
$\Delta V = 0.043$V, $\Delta i_1 = \Delta i_2 = 1.8$A, Tdown = 6.6 us
$V_{SM1} = 6.3$V, $V_{SR1} = -6.3$V, $V_{SM2} = 12$V, $V_{SR2} = -6.3$V

Simulation Results: Figure.6 shows the simulation setup. All the switches used in simulation of proposed circuit are IRF-150. Fig. 7 shows the simulated waveforms and it is clear that the phase currents i_1 and i_2 are equal in magnitude and there is an automatic phase current balance and a ripple cancellation effect. The average current through first phase is 7.28 amperes with a peak-to-peak ripple of 1.8 amperes and that through second phase is 7.44 amperes with a peak-to-peak ripple of 1.8 amperes, which are close to theoretical results. Fig.7 also shows that average value of the output current is 14.75 amperes with a peak-to-peak ripple of 1.08 amperes, which is close to theoretical result. The average value of the output voltage is 1.48 volts with ape peak-to-peak ripple of 0.042 volt and is close to theoretical results. The maximum voltage across switch SM_1 is 6.57 volts and that across SR_1 is -6 volts, which are close to theoretical results of 6.3 volts and -6.3 volts. The maximum voltage across SM_2 is 12 volts and that across SR_2 is -5.81 volts, which are also close to theoretical results of 12 volts and -6.3 volts. The small difference between theoretical and simulation results is due to the factor that the switching used in the simulation setup are not ideal.

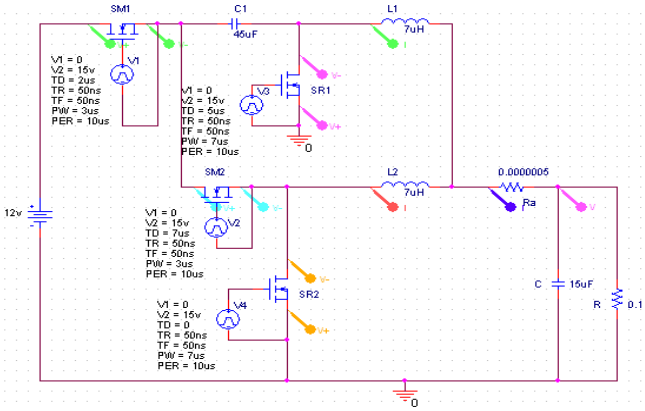

Fig. 6: Pspice schematic of proposed VRM in steady state

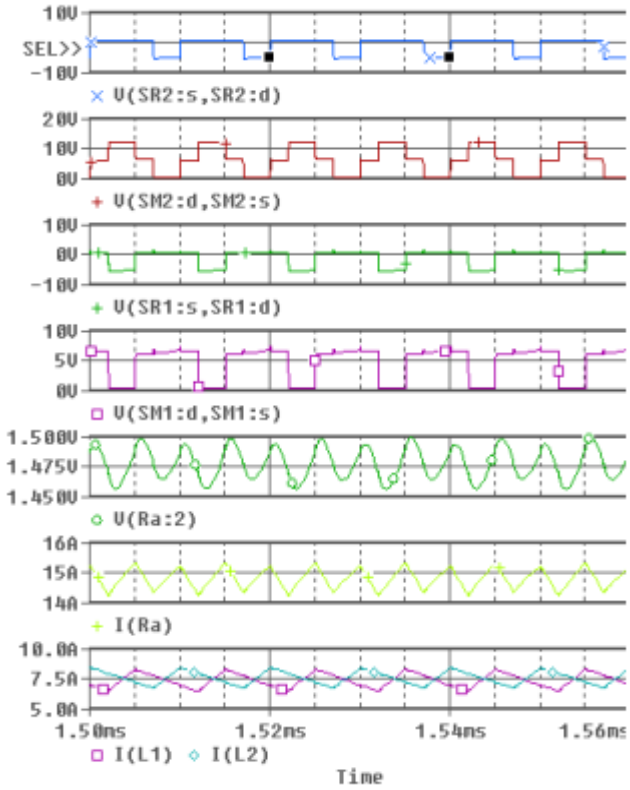

Fig. 7: Simulation Waveforms in steady state

Now for transient condition, the simulation setup is shown in Fig. 8.

For transient simulation two resistances in addition with a switch are used. The switch S_3 across the load resistor is on from time 0 to 1.6 ms. The equivalent load resistance R during this interval is equal to 0.1 ohm and can be calculated from R_1+ R_2 // R_{S3}. Where R_{S3} is the on-resistance of switch S_3 and its value is 0.055 Ω. Transient will be created at time t=1.6 ms by opening the switch S_3 and changing the load resistance from 0.1 ohm to 0.4 ohm, as a result of which output current will decrease from 14.75A to 4.4A and the output voltage jumps to an overshoot of 3.2 volts. Fig. 9 shows the simulation waveforms in load transient condition.

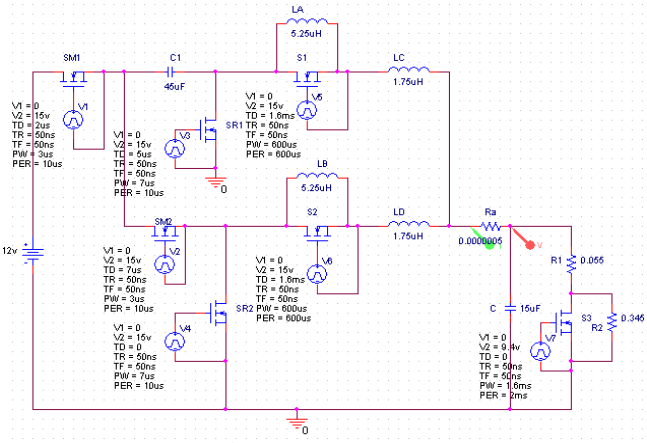

Fig. 8: Pspice schematic of proposed VRM in transient condition

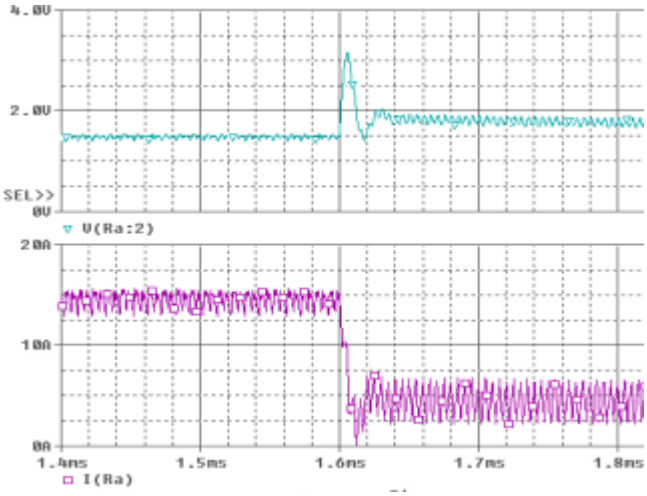

Fig. 9: Simulation Waveforms in Transient State

As shown in Fig. 9, the time taken by the output current to decrease from 14.75 amperes to 4.4 amperes is about 8us, and it is the same time required by the proposed VRM to recover its voltage overshoot from 3.2 volts to its normal value. These results are also close to theoretical results.

Simulation of both the synchronous rectifier VRM and two-phase VRM has also been carried out to compare their results with switched-inductor VRM. Fig. 10 shows the simulation waveforms of synchronous rectifier VRM and the simulation waveforms of two-phase VRM are shown in Fig. 11.

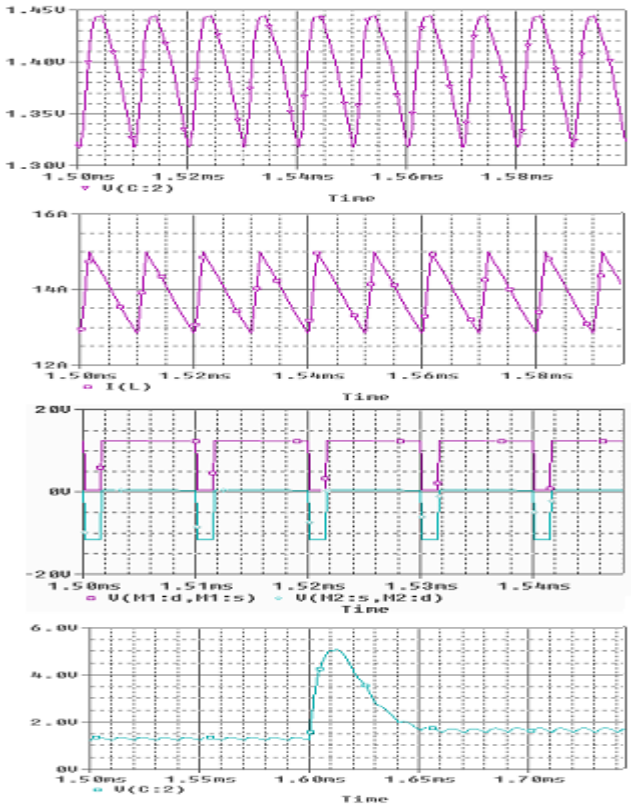

Fig. 10: Simulation Waveforms of Synchronous Rectifier VRM

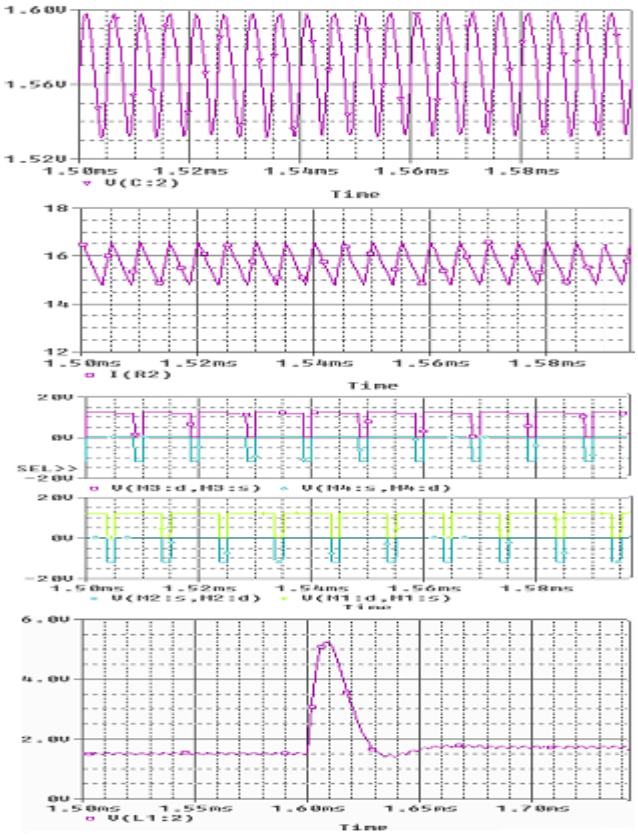

Fig. 11: Simulation Waveforms of Two-Phase VRM

3. Performance Comparison

To demonstrate the advantages of switched-inductor VRM, simulations are also done for conventional synchronous rectifier VRM and two-phase VRM. For a fair comparison, the same specifications (filter elements, input and output voltage) which have been used for obtaining the results of proposed VRM are used here to obtain theoretical and simulation results of these two conventional VRMs. The simulation results are analyzed thoroughly and table. I is generated for a better comparison purpose.

Table I: Comparison of Results

Parameters	Proposed VRM	Synchronous Rectifier VRM	Two-Phase VRM
D	0.3	0.15	0.15
Δi	1.03 A	2.18 A	1.8 A
ΔV	0.043 V	0.184 V	0.075 V
Tdown	6.6 µs	52.5 µs	26.25 µs
V_{SM1}(stress)	6.3 V	12 V	12 V
V_{SR1}(stress)	- 6.3 V	- 12 V	- 12 V
V_{SM2}(stress)	12 V	Not used	12 V
V_{SR2}(stress)	- 6.3 V	Not used	- 12 V

For the same design specifications, the switched-inductor VRM gives an output voltage of 1.8 volts at a duty ratio of 0.3, whereas both the conventional synchronous rectifier VRM and two-phase VRM gives the same output at a duty ratio of 0.15. Hence, the duty ratio of proposed VRM is extended to a double value. For a same amount of decrease in the load current, that is 13.5 ampere, the time taken by the proposed VRM to recover the voltage overshoot is 6.6 us, whereas synchronous rectifier VRM takes 52.5 us and the two-phase VRM takes 26.24 us to recover their voltage overshoots. Hence, the transient response of the proposed VRM is very fast. For same input voltage source of 12 volts, the voltage stress of the switches of proposed VRM is around 6 volts, and that of the switches of the synchronous rectifier VRM and two-phase VRM is 12 volts. This shows that the voltage stress of switches of proposed VRM is reduced to half.

Moreover, for same filter elements, the peak-to-peak ripple in the output current of proposed VRM is 1.03 ampere and the peak-to-peak ripple in its output voltage is 0.043 volt, whereas the peak-to-peak ripple in output current and voltage of synchronous rectifier are 2.18 ampere and 0.184

volt and that in the output current and voltage of two-phase VRM are 1.8 ampere and 0.075 volt. Hence, the peak-to-peak ripple in the proposed VRM is reduced. The reduced voltage stress (reduced switching loss) and reduced ripple in the proposed VRM improves its efficiency, as small ripple results in reduction of losses. The ripple in synchronous rectifier VRM and two-phase VRM can be reduced to that of proposed VRM by operating them at high switching frequency. However, this will decrease their efficiency due to increased switching losses. Moreover, these two VRMs operate on small duty ratio, which limits the use of higher switching frequencies.

4. Conclusions

A new topology of voltage regulator module (VRM) has been successfully designed for microprocessor applications. Due to automatic phase current balance, the phase currents are equal during the entire operation and the voltage stresses of switches are also reduced. The proposed VRM reduces the filter inductor in each phase to a quarter value during the load transient condition and the transient response of the proposed VRM is improved to a great extent. Complete analysis of switched-inductor VRM over all switching intervals is done and expressions for various variables have been derived. With reduced voltage stress of switches and with reduced output current ripple, the efficiency of switched-inductor VRM is improved. A comparator window is used in control loop to turn the switches S_1 and S_2 on and short the inductors only in load transient conditions. Theoretical results are obtained for both proposed VRM and two conventional VRMs by using suitable design parameters. These results show that the proposed VRM is better in performance than the conventional ones. Finally, theoretical results are verified by simulation in Pspice. The simulation results agree theoretical results. The proposed VRM has fast transient response and is well suited for present and future microprocessors.

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