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Optimized design of Carry Skip BCD adder using new FHNG reversible logic gates

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Abstract

Reversible logic is very essential for the construction of low power, low loss computational structures which are very essential for the construction of arithmetic circuits used in quantum computation, nanotechnology and other low power digital circuits. In the present paper an optimized and low quantum cost one digit carry skip BCD adder using new reversible logic gates are proposed. The proposed work is best compared to the other existing circuits.

Keywords*: Reversible logic, Reversible gate, Carry skip BCD adder, Quantum computing, Quantum cost, nanotechnology based systems.*

1. Introduction

Reversible logic has received great attention in the recent years due to its ability to reduce the power dissipation. Quantum arithmetic components need reversible logic circuits for their construction. Reversible logic circuits find wide application in low power digital design, quantum computing and nanotechnology. In 1960 R.Landauer demonstrated that high technology circuits and systems constructed using irreversible hardware results in energy dissipation due to information loss. According to Landauer's principle, the loss of one bit of information dissipates kTln2 joules of energy where k is the Boltzmann's constant and T is the absolute temperature at which the operation is performed [1]. Later Bennett, in 1973, showed that in order to avoid kTln2 joules of energy dissipation in a circuit it must be built from reversible circuits [2]. A reversible logic gate is an n-input, n-output logic device with one-to-one mapping. Reversible circuits are constructed using reversible logic gates. These reversible circuits not only produce unique output vector from each input vector but also the input can be reconstructed from the outputs. A reversible circuit should be designed using a minimum number of reversible gates. Fan-out and loops are not allowed in reversible logic circuits [3]. However fan-out and feedback can be achieved by using additional gates.

The complexity and performance of the circuit is decided on the following parameters [4, 5 and 7].

1. Garbage outputs: The number of unused outputs present in the reversible logic circuit.
2. Number of reversible gates: Total number of reversible gates used in the circuit.
3. Constant inputs: The number of inputs which are maintained constant at 0 or 1 in order to get the required function. They are necessary to synthesize a reversible function.
4. Quantum cost: The number of 1x1 or 2 x 2 reversible logic gates used in the quantum equivalent of the reversible circuit.

The synthesis of a reversible logic circuit should have following optimization parameters [4-18]:

1. Minimum number of gates
2. Minimum number of garbage outputs
3. Minimum number of constant inputs
4. Minimum number of quantum costs

Decimal addition plays an important role in various microprocessors and other future computing circuits.

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Therefore circuits designed to perform decimal addition using binary methods must be fast and must incorporate the required correction to produce accurate decimal sum. The present paper proposes an optimized design of a carry skip BCD adder using new reversible logic gates. The proposed one digit carry skip BCD adder is constructed using a minimum number of reversible logic gates and it produces the least number of garbage outputs, minimum number Quantum cost compared to other existing circuits and therefore it can used to build more complex arithmetic circuits using reversible logic gates.

This paper is organized as follows: Section 2 gives the brief introduction to some of the important basic reversible logic gates. In Section 3 the new gates used in the proposed design of carry skip BCD adder circuits are explained. In Section 4, the conventional one digit carry skip BCD adder circuit and its implementation using new reversible gates are described. Section 5 gives the reversible logic implementation of the proposed designs of these adders. Section 6 gives the results and discussion and also the comparison of proposed design with other existing circuits. Finally Section 7 concludes with a scope for further research.

2. Literature Review

At present there are many 3x3 reversible logic gates such as Fredkin gate, Toffoli gate, Double Feynman gate, Peres gate [3-8]. The quantum cost of each reversible logic gate is an important optimization parameter [7].The quantum cost of a 1x1 reversible gate is assumed to be zero. The quantum cost of a 2x2 reversible logic gate is taken as unity. The quantum cost of other reversible gates is calculated by counting the number of V, V^+ and CNOT gates present in their quantum circuit. V is the square root of NOT gate and V^+ is its hermitian. The V and V^+ quantum gates have the following properties:

$V * V = NOT$ (1)
$V * V^+ = V^+ * V = 1$ (2)
$V^+ * V^+ = NOT$ (3)

Important reversible logic gates are,

2.1. Feynman gate

Figure 1 shows a 2 x2 Feynman gate [3]. The input vector is I (A, B) and the output vector is O (P, Q) and the relation between input and output is given by

$P=A$, $Q = A \oplus B$. Since it is a 2 x 2 gate, it has a quantum cost of **1** [8]. It is used to copy the input without producing garbage bits.
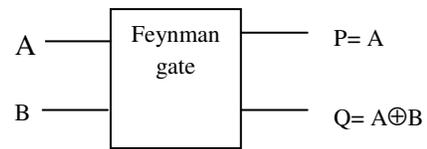
Figure .1 Feynman gate

2.2. Double Feynman gate (F2G)

Figure 2 shows a 3 x 3 Double Feynman gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q, R) and output is defined by P = A, Q = $A \oplus B$, R = $A \oplus C$. Quantum cost of Double Feynman gate is **2**.
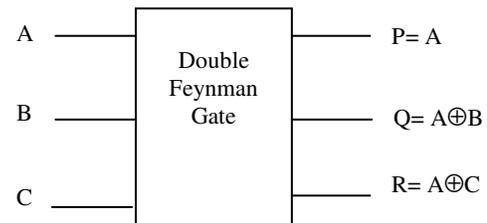
Figure .2 Double Feynman gate

2.3. Toffoli gate (TG)

Figure 3 shows a 3 x 3 Toffoli gate [5]. The input vector is I (A, B, C) and the output vector is O (P, Q, R) and output is defined by P = A, Q = B, R = $AB \oplus C$. Quantum cost of a Toffoli gate is **5**.
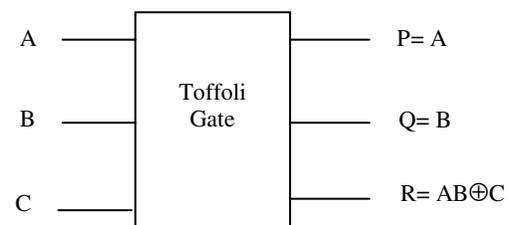
Figure.3 Toffoli gate

2.4. Fredkin Gate (FG)

Figure 4 shows a 3 x 3 Fredkin gate [4]. The input vector is I (A, B, C) and the output vector is O (P, Q and R). The output is defined by P=A, Q=$A'B \oplus AC$ and R=$A'C \oplus AB$. Quantum cost of a Fredkin gate is **5**.

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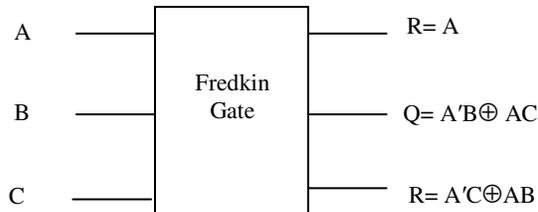
Figure.4 Fredkin gate

2.5. Peres Gate (PG)

Figure 5 shows a 3x3 Peres gate [6]. The input vector is I (A, B, C) and the output vector is O (P, Q and R). The output is defined by $P = A$, $Q = A \oplus B$ and $R = AB \oplus C$. Quantum cost of a Peres gate is 4.
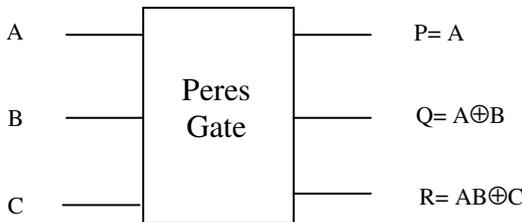
Figure.5 Peres gate

2.6. HNG gate

Figure 6 shows a HNG Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). $P = A$, $Q = B$, $R = A \oplus B \oplus C$ and $S = (A \oplus B) C \oplus AB \oplus D$. The full adder using HNG is obtained with $C = C_{in}$ and $D = 0$ and its quantum cost is equal to 6.
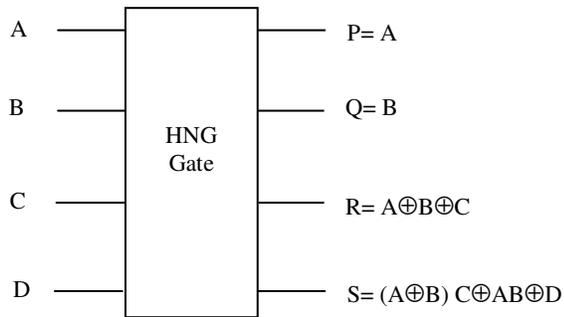
Figure.6 HNG Gate

2.7. TSG gate

Figure 7 shows a TSG Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). $P = A$, $Q = A'C' \oplus B'$, $R = (A'C \oplus B') \oplus D$ and $S = (A'C' \oplus B') D \oplus (AB \oplus C)$. The full adder using DPG is obtained with $C = 0$ and $D = C_{in}$ and its quantum cost is equal to 13.
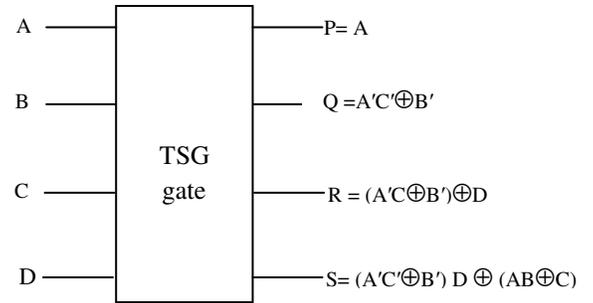
Figure.7 TSG Gate

2.8. MKG gate

Figure 8 shows a MKG Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q and R, S). $P = A$, $Q = C$, $R = (A'D' \oplus B') \oplus C$ and $S = (A'D' \oplus B') C \oplus (AB \oplus D)$. The full adder using DPG is obtained with $C = C_{in}$ and $D = 0$ and its quantum cost is equal to 14.
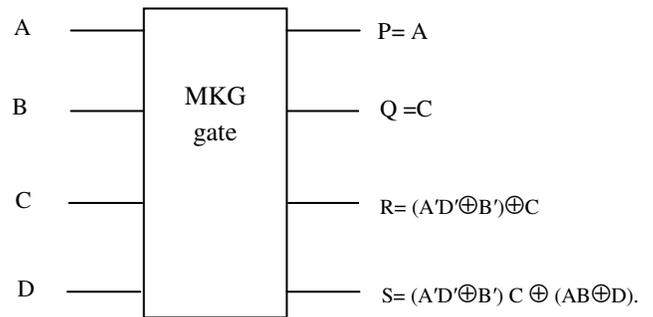
Figure. 8 MKG Gate

2.9. Double Peres gate (DPG)

Figure 9 shows a Double Peres Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S). $P = A$, $Q = A \oplus B$, $R = A \oplus B \oplus D$ and $S = (A \oplus B) D \oplus AB \oplus C$. The full adder using DPG is obtained with $C = 0$ and $D = C_{in}$ and its quantum cost is equal to 8.
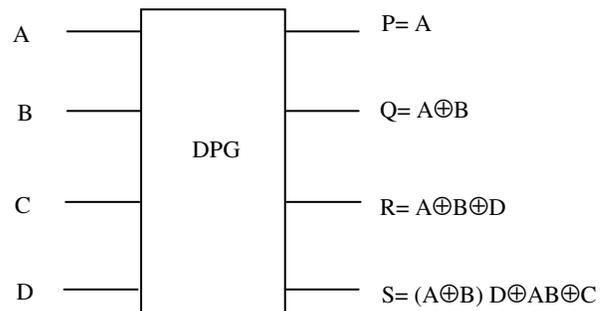
Figure.9 Double Peres gate.

2.10. SCL gate (SCLG)

Figure 10 shows a 4 x 4 SCL gate [12]. The input vector is I (A, B, C, D) and the output vector is O(P,Q,R,S) and the relation between input and output is given by,
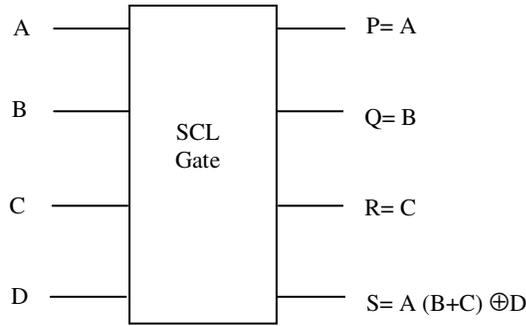
Figure.10 Six-correction logic gates

There is a one-to-one mapping between inputs and outputs of SCL gate and it can be used to add 6 to the sum in order to correct it to get the correct BCD sum [12].In the present paper SCL gate (Six Correction Logic) is used for the required correction in the BCD addition. In a BCD adder, the correction logic which generates the C_{out} is given by,

$$C_{out} = S_3S_2 + S_3S_1 + C_4 \qquad (4)$$

The above equation can also be expressed without changing its functionality into,

$$C_{out} = C_4 \oplus S_3 (S_2 + S_1) \qquad (5)$$

The proposed SCL gate gives the required correction logic at the output S=C_{out} and also passes the inputs A= S_3, B=S_2 and C=S_1 to P, Q and R respectively as shown in fig.11,thereby avoiding the fan-out problem present in the BCD adder and carry skip adder circuit given in the paper [14-17].
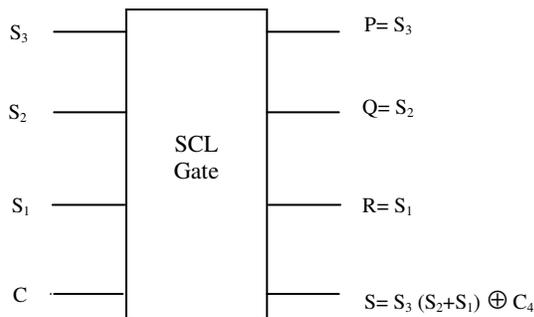
Figure.11 SCL gate producing C_{out}

3. Proposed Reversible Gates

3.1. FHNG gate

Figure 12 shows a FHNG Gate. The input vector is I (A, B, C, D) and the output vector is O (P, Q, R, S).P =A, Q =A⊕B, R =A⊕B⊕C and S= (A⊕B) C⊕AB⊕D. The full adder using FHNG is obtained with C= C_{in} and D=0 and its quantum cost is equal to 7.Let
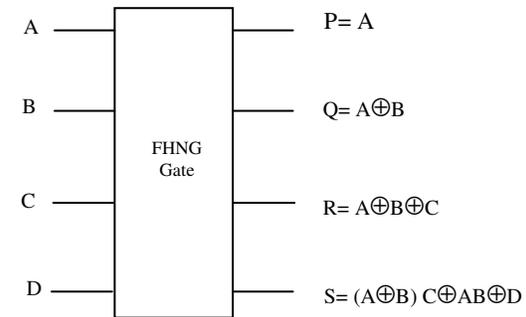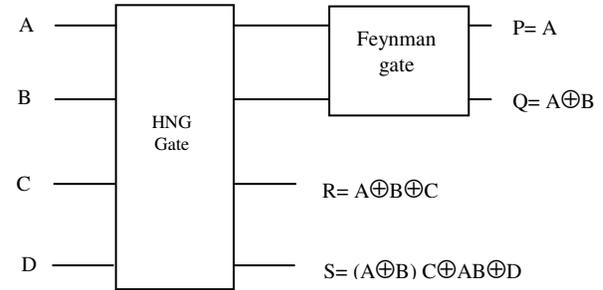
Figure.12 FHNG Gate

Table 1: Truth table of proposed reversible FHNG gate

A	B	C	D	P	Q	R	S
0	0	0	0	0	0	0	0
0	0	0	1	0	0	0	1
0	0	1	0	0	0	1	0
0	0	1	1	0	0	1	1
0	1	0	0	0	1	1	0
0	1	0	1	0	1	1	1
0	1	1	0	0	1	0	1
0	1	1	1	0	1	0	0
1	0	0	0	1	1	1	0
1	0	0	1	1	1	1	1
1	0	1	0	1	1	0	1
1	0	1	1	1	1	0	0
1	1	0	0	1	0	0	1
1	1	0	1	1	0	0	0
1	1	1	0	1	0	1	1
1	1	1	1	1	0	1	0

4. Conventional Carry Skip BCD Adder

4.1. Conventional Carry Skip Adder

The circuit is as shown in fig 10. It uses two four bit adders, carry skip logic circuit and a correction logic circuit. The carry skip BCD adder is faster than the above BCD adder as it skips the propagation of carry input if Z=1. The carry propagate input $Z = Z_0.Z_1.Z_2.Z_3$ is generated at the output of a 4-input AND gate where $Z_0 = (A_0 \oplus B_0)$, $Z_1 = (A_1 \oplus B_1)$, $Z_2 = (A_2 \oplus B_2)$ and $Z_3 = (A_3 \oplus B^3)$. When Z=1, the carry input C_{in} is propagated to reach C_{out}, otherwise it is skipped without propagating through the full adders. If Z=0, C_4 is propagated to C_{out}. Also whenever $C_{out} = 1$, correction logic adds 6 to the sum to generate the correct BCD sum as per rules of BCD addition.
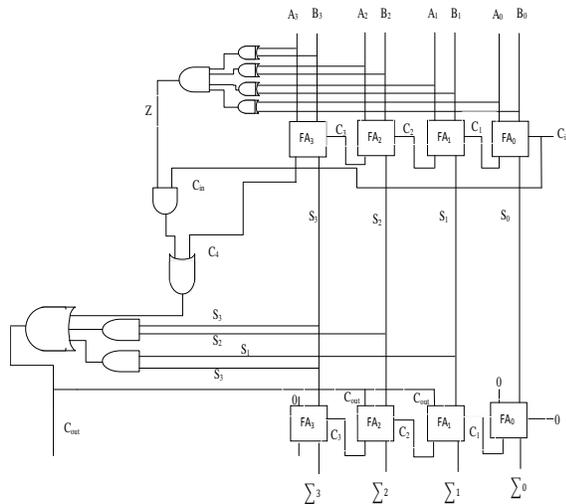
Figure.13 One digit Carry skip BCD adder

5. Reversible Logic Implementation of Carry Skip BCD Adder

One digit Carry skip BCD adder using reversible logic gates the circuit can be divided into three blocks.

1. Adder-1 and XOR-AND4 block which outputs C_{in}, C_4, Z along with S_3, S_2, S_1 and Σ_0 shown in fig .13 and is represented in this paper as a single block shown in fig.14.
2. AND-OR and Correction logic circuit block which outputs $P = Z_{Cin} + C_4$ and $C_{out} = P \oplus S3 (S_2 + S_1)$ shown in fig 15.
3. Adder-2 block which adds 110 to S3, S2 and S1 whenever $C_{out} = 1$ and outputs the corrected BCD $\Sigma_3 \Sigma_2 \Sigma_1 \Sigma_0$ shown in fig 16.
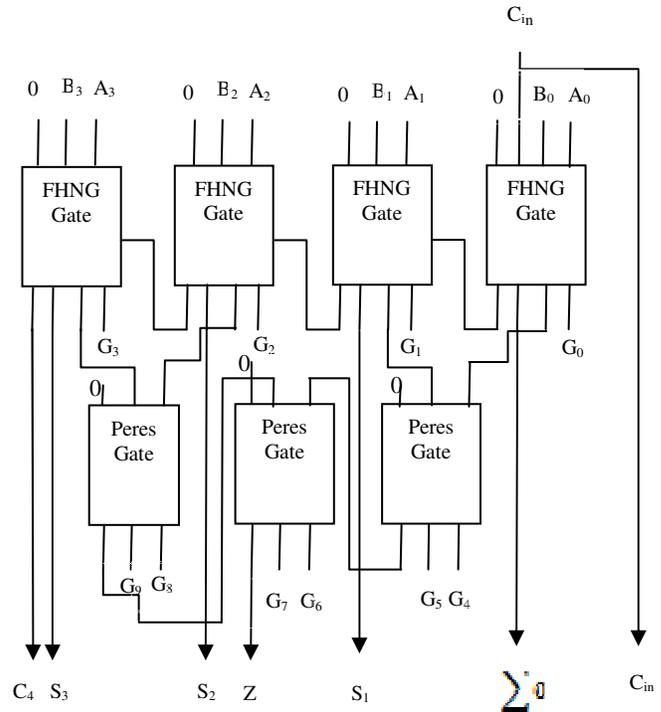
Fig.14 BLOCK-1 (Adder-1 and XOR-AND4)
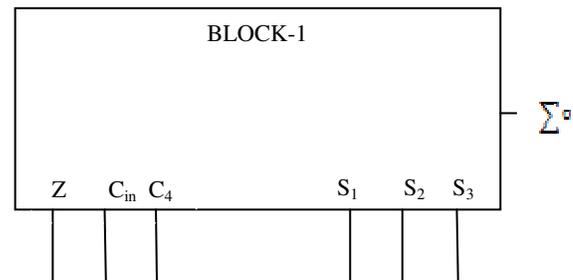
Figure.15 BLOCK-1(Adder-1 and XOR-AND4)
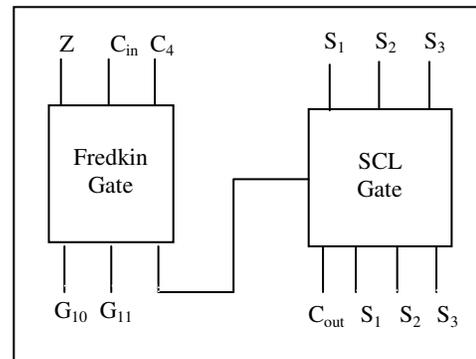
Figure.16. BLOCK-2(AND-OR and Correction logic circuit)

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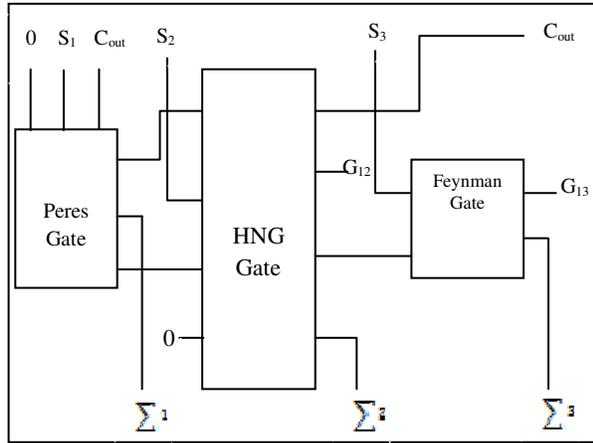
Figure.17. BLOCK-3 (Adder-2)

The proposed optimized circuit of a Carry skip BCD adder is as shown in fig 18.
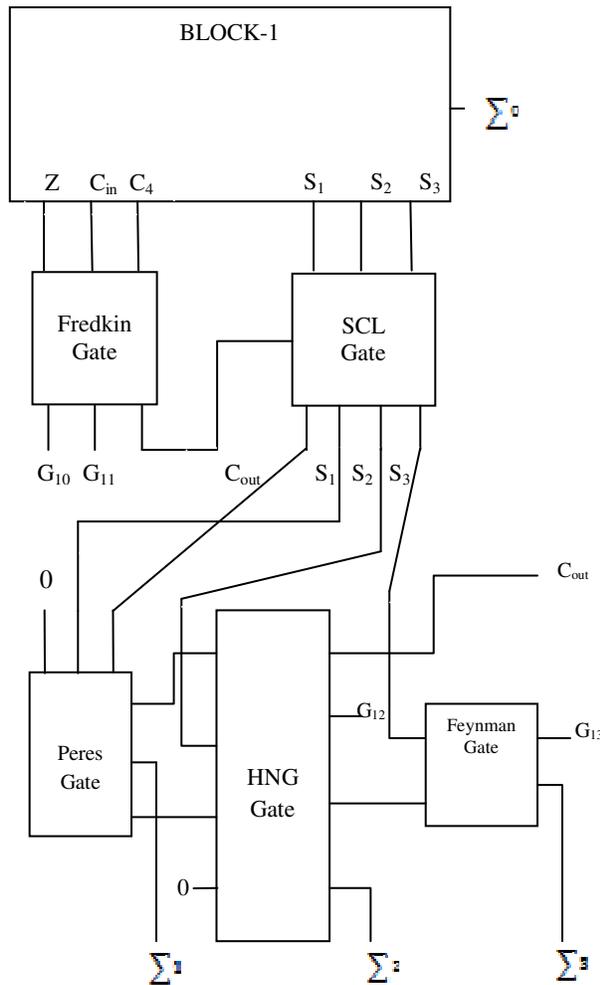
Figure.18. Optimized Carry skip BCD adder circuit

5.1. Design Details of Carry Skip BCD Adder

Four bit parallel adder
The 4 bit parallel adder is constructed using FHNG gates since it has lowest quantum cost and it is 7. Also the XOR of the operand bits is readily available at one of its output which is very much required for the generation of carry propagate signal. So the total number of garbage outputs from the adder is only 4.

XOR gates and an AND gate
In the present circuit the function of four XOR gates is achieved without using any extra reversible gates since the XOR of the operands is available at the outputs of the FHNG adder block. This produces 4 garbage outputs from the adder block. However the AND of these Z_0, Z_1, Z_2 and Z_3 is obtained by using three Peres gates. The quantum cost is reduced it is known that the quantum cost of a Peres gate is 4 [6, 19].

OR gate and an AND gate block
AND-OR of Z C_{in} and C_4 is obtained using a Fredkin gate which outputs $P = ZC_{in}+C_4$.OR gate and an AND

C_{out} generation
This is generated using a new gate SCL gate which outputs $C_{out} = P \oplus S_3 (S_2 + S_1)$ along with S_3, S_2 and S_1. These can be used as inputs to the next gates to correct the BCD sum.

Also the second adder which should add six in order to correct and convert the sum to BCD sum need not be a 4bit parallel adder but instead it can be constructed using one Peres gate, one HNG gate and one Feynman gate similar to the existing designs [16-17, 20, 22]. The Peres gate is used to add S_1 with C_{out} to produce final Σ_1 and a carry which is given to one HNG gate used as a full adder to produce final Σ_2. Then the final sum bit Σ_3 is obtained by using one Feynman gate. So the BCD sum is $\Sigma_3 \Sigma_2 \Sigma_1 \Sigma_0$.

6. Results and Discussion

6.1. Carry Skip BCD Adder

Several designs existing in the literature are discussed and compared with the proposed design [14-16].In [14] 3 New gates [NG] for the correction logic circuit and 8 TSG gates for the adders (for both adder-1 and adder-2 blocks) are used for the construction of reversible implementation of BCD adder. This reduces the number of gates but in this paper fan-out is not taken into account which when considered will

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increase the number of gates more than 15. This produces 27 garbage outputs with 11 constant inputs. The multiple fan-outs are not permitted in the synthesis of a reversible logic circuit.

In [15] BCD adder is constructed using 23 reversible gates. One bit Full adder cell is realized using one NG and one PG gate which produce 2 garbage outputs. So a 4bit adder produces 8 garbage outputs and requires 8 reversible logic gates. The six correction logic is obtained using 3 TG with six garbage outputs. Also, it uses 4 FG for fan-out purpose. So the circuit of [15] uses a total of 23 reversible logic gates with 22 garbage outputs.

In [16] BCD adder is constructed using 23 reversible gates. One bit Full adder cell is realized using one NG and one NTG gate which produce 2 garbage outputs. So a 4bit adder produces 8 garbage outputs and requires 8 3*3 reversible logic gates. The six correction logic is obtained using three NG with six garbage outputs. Also it uses 4 FG far fan-out purpose. The circuit of [16] uses a total of 23 reversible logic gates with 22 garbage outputs and requires 17 constant inputs.

The implementation given in [19] uses two Fredkin gates and one Toffoli gate for the correction logic and also it uses a 4bit parallel adder constructed using four MTSGs. It also uses a combination of one FG, one PG and a MTSG for the adder-2 block which adds the c_{out} to the sum in order to generate the final BCD sum. Also to generate block generation bit P three FRGs are used. Finally to generate c_{out} and to fan-out three sum bits another three FRGs and a TG are used. This implementation requires a total of 15 reversible logic gates and it produces a total number of 14 garbage outputs (including the garbage from the correction circuit) with 11 constant inputs with a delay of 10 units. The advantage of using this design over that given in [18] is that the quantum cost of MTSG is less than the quantum cost of TSG [19].

The implementation given in [22] uses four DPG gates and three PG gates to construct the adder-1 and XOR-AND4 block that means 4bit parallel adder. It also uses a combination of one Fredkin Gate, one SCL gate to create AND-OR and Correction logic circuit block. The adder-2 has one PG gate one DPG gate and one FG gate. This implementation requires a total of 13 reversible logic gates and it produces a total number of 14 garbage outputs (including the garbage from the correction circuit) with 10 constant inputs with the quantum cost is 63(the quantum cost of SCL gate is undefined).

The proposed design uses a FHNG gate whose quantum cost is 7. The number of reversible logic gates used in the proposed design is reduced to 12 which are minimum as compared to the other existing designs. This produces 13 garbage outputs with 9 constant inputs and the quantum cost is 56(the quantum cost of SCL gate is undefined). So it is observed that the proposed design is a much optimized circuit than the existing ones. The comparative studies of various designs of carry skip BCD adders are presented in Table-2.

Table 2: Comparison of Carry skips BCD adders

Carry skip BCD adder	No of gates	No of garbage output	Constant inputs	Quantum cost
Paper(14)	15	27	15	Undefined
Paper(18)	15	14	11	Undefined
Paper(19)	15	14	11	Undefined
HNG gate	16	13	10	Undefined
Paper(22)	13	14	10	63
Proposed Design	12	13	9	56

7. Conclusions

In this paper an optimized one digit carry skip BCD adder are presented. The design is very useful for future computing techniques like ultra low power digital circuits and quantum computers. It is shown that the proposal is highly optimized in terms of the number of reversible logic gates, the number of garbage outputs and the quantum cost. The analysis of various implementations discussed is tabulated in Table-II. It gives the comparison of the different designs in terms of the important design parameters like the number of reversible gates, number of garbage outputs, and the number of constant inputs and the quantum cost. From the table it is observed that the present proposal uses the least number of gates producing the least number of garbage outputs and has the minimum quantum cost compared to other design methods. Also the design uses FHNG gates for the construction of adders which greatly reduces the total cost of the circuit. Because of these optimization parameters the overall cost of the circuit will be reduced. Using this one digit Carry skip BCD

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adder, N-digit Carry skip BCD adders can be constructed. The design method is definitely useful for the construction of future computers and other computational structures. Optimization of other computational circuits is under investigation as a future work.

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