Proposal of a New High Step-Up Hybrid Switch Converter with Reduced Switch Voltage Stress

Muhammad Saleem[1], Obaid Rehman[1] and Hashmat Khan[1]

[1]Department of Electrical Engineering, Sarhad University of Science and Information Technology, KPK, Peshawar, Pakistan.

Abstract

In this paper a new step-up DC-to-DC converter with high voltage conversion ratio with small voltage stress is presented. The converter is suitable for the applications where high voltage conversion ratio is required. The proposed converter is different from the conventional Cuk converter and for a given duty ratio provides high conversion ratio with reduced switch voltage stress. Due to low switch voltage stress, the hybrid switch converter utilizes a MOSFET switch with low voltage rating and low on resistance. Hence it has low conduction loss and high efficiency. The principles of operation and the theoretical analysis are presented in this paper. In order to validate the theoretical results the proposed converter is simulated for 35 W prototype operating at 100 KHz.

Keywords: *DC-DC converters, voltage conversion ratio, switch voltage stress, duty ratio.*

1. Introduction

Many applications require high step-up, non-isolated DC-to-DC converters. Typical applications are renewable energy systems, fuel cells, and uninterruptible power supply (UPS) systems [1]. The duty ratio for conventional step up converter is high for high output voltage. In general converters with high voltage conversion ratios have some limitations namely high switch voltage stress and efficiency. So the existing converters with high voltage conversion ratios require research in term of efficiency and switch voltage stress.

Conventional boost converter with high output voltage requires MOSFET with high voltage ratings. Such MOSFET has a high on-resistance, which increase size, cost, and conduction losses [2].

A quadratic boost converter can provide high output voltage with a small duty ratio. However, high voltage across the switch in the off state and low efficiency are the main disadvantages of this converter [3].

A boost converter with a voltage doubler has been proposed in [4]. It gives high voltage conversion ratio. It operates as interleaved boost converter. Using constant frequency control, this topology provides voltage regulation. The voltage conversion ratio is four times that of a conventional non-isolated boost converter. However, the use of two switches and auxiliary transformer results in increase in cost, size and circuit complexity.

A boost converter has been proposed which uses a clamp mode coupled inductor with an active switch [5]. The converter achieves high efficiency due to the leakage energy recovered by the passive clamp circuit. It also avoids the reverse recovery problem of the output rectifier. High ripple in the input current and high magnitude clamp capacitor's current are the main disadvantages of this converter.

A switch-capacitor circuit has been combined with the conventional boost converter to get high step-up conversion ratio [6]. The switch capacitor circuit is made of two diodes, two capacitors and one controlled switch. This converter has many advantages as compared to the quadratic boost converter, namely low switch voltage stress and better efficiency. Due to low switch voltage stress, it uses MOSFET with low voltage rating.

Another idea of the switch-capacitor circuit has been applied to conventional Cuk, zeta and single-ended primary inductance converter (SEPIC) converters [7].. These converters provide high efficiencies and low switch voltage stresses as compared to quadratic converters. The conversion ratios are smaller than quadratic converter. By increasing the number of capacitors, conversion ratio can be increased with small penalty on conduction losses.

A switch capacitor technique has been used to increase the input voltage to the required output voltage level [8], [9]. A switch capacitor circuit is inserted within a boost converter. It achieves high voltage conversion ratio with low duty ratio. High efficiency is the main advantage of this converter. The major drawback of this converter is high switch voltage stress.

A new converter has been presented in [10]. The proposed topology provide very high voltage conversion ratio with low duty ratio. The major draw back of this converter is the pulsating output current.

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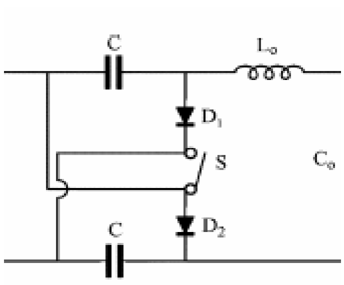
A new idea of DC-to-DC converters has been presented in [2]. The converters in this class utilize a new high step up switch cell made of two capacitors, two diodes and a single switch. High voltage conversion ratios, low voltage stresses and small sizes are attractive features of these converters.

2. Proposed Hybrid Switch Converter

This hybrid switch converter is based on the use of new switching cell. This new switching cell is combines the idea of two switching cells. One of the two switching cell is presented in [2], which consists of two diodes, two identical capacitors, one inductor and one switch as given in Fig.1 (a). The second switching cell is presented in [10] consists of three diodes and two identical capacitors as given in Fig. 1(b). The new switching cell is obtained by replacing output inductor in the switching cell of Fig.1.(a) with a diode D_3 as given Fig. 1(c). The purpose of replacing the output inductor L_o with a diode D_3 is to increase voltage conversion ratio and to reduce switch voltage stress. Replacement of intermediate capacitor, output inductor and output diode of conventional Cuk converter with the new switching cell leads to hybrid switch converter as given Fig. 1(d).

Due to low switch voltage stress, the hybrid switch converter utilizes a MOSFET switch with low voltage rating and low on resistance. Hence it has low conduction loss and high efficiency



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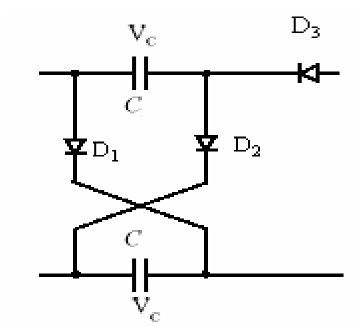

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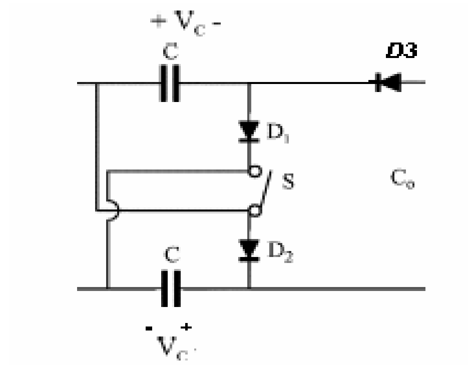

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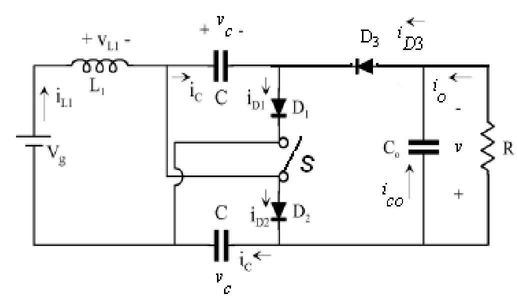

(d)

Fig.1. (a) Four terminal high step-up cell (b) Inverting SC cell (c) Proposed cell (d) Proposed Hybrid switch converter

2.1 Principles of Operation

For the analysis of the converter it is assumed that the converter is operating in the steady state and following assumption are made during one switching cycle. It is assumed that all the components are ideal. The capacitors and inductor are so sized to have negligible voltage ripple and inductor current ripple respectively.
Operation of hybrid switch converter can be explained in two switching intervals.

Stage 1[0, DTs], Fig 2(a): During first switching interval when switch S is closed, diodes D_1 and D_2 are reverse biased due to the negative voltage of capacitor "-V_c" and D_3 is forward biased. During this interval the voltage across series capacitors are equal. Both series capacitors 'C' charging the load and output capacitor 'C_o'. The energy is stored by inductor in this interval.

Stage 1[DTs, Ts], Fig 2(b): During second switching interval when the switch is open, diodes D_1, D_2 are forward biased and output diod D_3 is reversed biased. In this interval the two capacitors 'C' are in parallel. In this interval the two capacitors 'C' are equally charged. Current through each diode D_1, D_2 are equal having magnitudes equal to $i_{L1}/2$. Output capacitor 'C_o' is discharged into load R to supply load current.

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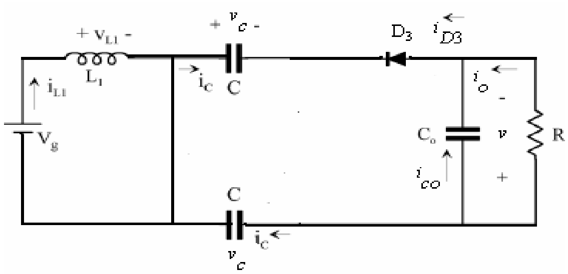
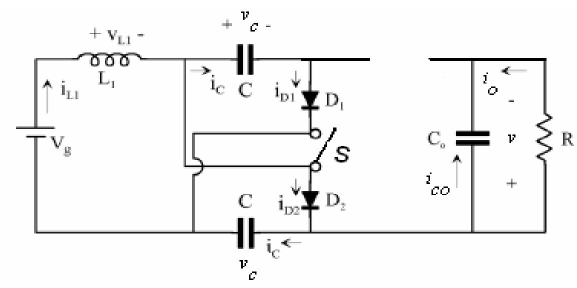


(a)



(b)

Fig. 2 (a) First switching interval (b) Second switching interval

For first switching interval ($0 \le t \le DT_s$)

$$v_{L1} = L_1 \frac{di_{L1}}{dt} = V_g \tag{1}$$

$$i_{co} = C_{co} \frac{dv}{dt} = \frac{(1-D)}{2D} i_{L1} - i_o \tag{2}$$

$$i_c = C \frac{dv_c}{dt} = -\frac{D^{/}}{2DC} I_{L1} \tag{3}$$

For second switching interval ($DT_s \le t \le T_s$)

$$v_{L1} = L_1 \frac{di_{L1}}{dt} = V_g - v_c \tag{4}$$

$$i_{co} = C_{co} \frac{dv}{dt} = -i_o \tag{5}$$

$$i_c = \frac{i_{L1}}{2} \tag{6}$$

2.2 Voltage Conversion Ratio and Switch Voltage Stress

By the application of small ripple approximation and Principles of inductor volt-second balance, the expression for the voltage conversion ratio is obtained.

$$M = \frac{V}{V_g} = \frac{2}{1-D} \tag{7}$$

For normalized switch stress

$$M_s = \frac{1}{2}$$

The voltage stress is half of the output voltage which is less than conventional Cuk converter. Th voltage stress is independent of the duty cycle.
Using Principles of Capacitor Charge Balance following equation is obtained:

$$I_{L1} = \frac{2I_o}{D^{/}} \tag{8}$$

where $D^{/} = 1-D$

2.3 Inductor Design

Using the expression (1) and the time interval during first switching interval, inductor current ripple 'Δi_{L1}' is equal to

$$L_1 = \frac{V_g}{2\Delta i_{L1}} DTs \tag{9}$$

2.4 Series Capacitor Design

The size of capacitor is selected according to voltage ripple in the capacitor. Greater is the value of capacitance, smaller will be the ripple. Using the expression (3) and the time interval during first switching interval, the series capacitor voltage ripple is equal to

$$C = \frac{I_o T_s}{2\Delta v_c} \tag{10}$$

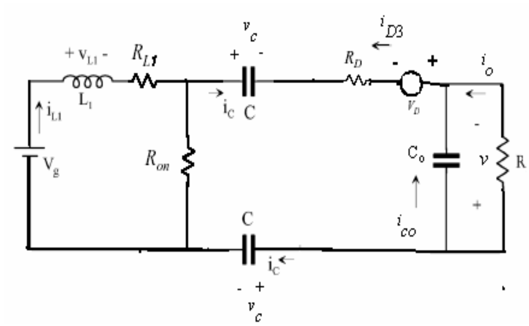
2.5 Output Capacitor Design

Using the expression (5) and the time interval during first switching interval, the output capacitor voltage ripple is equal to

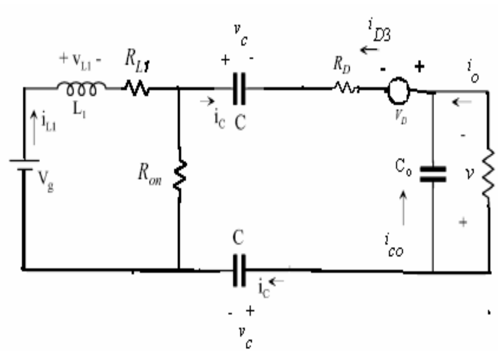
$$C_0 = \frac{I_o (1-D)Ts}{2\Delta v} \tag{11}$$

2.6 Converter Efficiency

Practical inductor is modeled by a resistor R_{L1} which is connected in series with inductor. Copper loss occur due to the internal resistance of inductor which is modeled by R_{L1}. Similarly R_{on} represents the on resistance of MOSFET. The forward voltage drop occurs in MOSFET due this resistance. This on resistance is the major source of power loss in semiconductor devices. Actual diode is modeled by voltage source V_D plus diode on resistance R_D.



(a)



(b)

Fig. 3. (a) First switching interval (b) Second switching interval

For $(0 \le t \le DT_s)$

$$v_{L1} = V_g - i_{L1}(R_{L1} + R_{on}) - i_{D3}R_{on}$$

For $(DTs \le t \le T_s)$

$$v_{L1} = V_g - v_C - V_D - i_{L1}R_{L1} - \frac{i_{L1}}{2}R_D$$

Since the average current through diode D_3 is equal to the average load current therefore

$$\langle i_{D3} \rangle = I_o$$

$$v_{L1} \approx V_g - I_{L1}(R_{L1}+R_{on}) - I_oR_{on}$$

$$v_{L1} \approx V_g - V_c - V_D - I_{L1}R_{L1} - \frac{I_{L1}}{2}R_D$$

$$v = 2v_c - V_D - (i_{L1} + i_o)R_{on}$$

Apply small ripple approximation

$$V = 2V_c - V_D - I_{L1}R_{on} - I_oR_{on}$$

Using inductor volt-second balance principle

$$D(V_g - I_{L1}(R_{L1}+R_{on}) - I_oR_{on}) +$$

$$(1-D)(V_g - V_c - V_D - I_{L1}R_{L1} - \frac{I_{L1}}{2}R_D) = 0$$

Putting the values of I_{L1} and V_c, we get

$$V = \frac{\frac{2Vg}{1-D} - 3V_D}{\frac{4DR_{on}}{(1-D)^2R} + \frac{4R_{L1}}{(1-D)^2R} + \frac{2DR_{on}}{(1-D)R} + \frac{2R_D}{(1-D)R} + \frac{2R_{on}}{(1-D)R} + \frac{R_{on}}{R} + \frac{R_D}{R} + 1}$$

$$\eta = \frac{(\frac{1-D}{2})\,(\frac{2}{1-D} - \frac{3V_D}{V_g})}{\frac{4DR_{on}}{(1-D)^2R} + \frac{4R_{L1}}{(1-D)^2R} + \frac{2DR_{on}}{(1-D)R} + \frac{2R_D}{(1-D)R} + \frac{2R_{on}}{(1-D)R} + \frac{R_{on}}{R} + \frac{R_D}{R} + 1}$$

3. Simulation Results

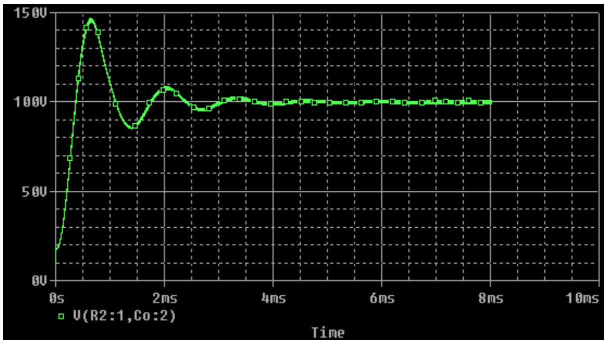
Circuit simulation test was conducted for the proposed hybrid switch converter using orcade simulator to validate theoretical results and to measure the performance of the proposed converter in term of voltage conversion ratio and switch voltage stress. The results of proposed converter were compared with type 1 Cuk topology Converter, non-inverting Zeta derived converter and inverting Zeta derived. The converter is simulated for the real application HID (high-intensity-discharge) lamp use in a car, whose specifications are:
V_g =12 V, V= 100 V, P_{out} =35 W.

The input inductor L_1 value is set to 156.34 μH to ensure the CCM operation where as the values of Series capacitor C and Output capacitor were set to 4.5μF and 1μF respectively.

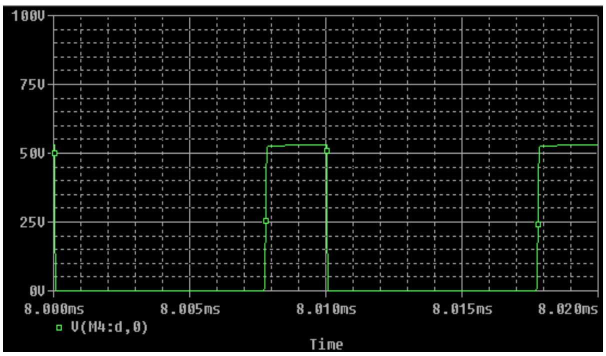
The simulated waveforms are shown given in fig. 4. It is clear from the simulation result that hybrid switch converter gives an output voltage of 100 volts at a duty ratio of 0.76 whereas the type 1 Cuk topology, non-inverting zeta-derived converter and inverting zeta-derived converter gives the same output voltage at a duty ratios 0.78, 0.78 and 0.86 of respectively. Hence the hybrid switch converter gives 100V output voltage at smaller duty ratio as compared to other converters. This shows that voltage conversion ratio of hybrid switch converter is higher as compare to other three converters.

Similarly, the switch voltage stress of hybrid switch converter is 52V where as the switch voltage stresses of type 1 Cuk topology, non-inverting zeta-derived converter and inverting zeta-derived converter are 58V, 59V and

94V respectively. So the switch voltage stress of hybrid switch converter is lower as compared to other three converters.



(a)



(b)

Fig. 4 (a) Output voltage (b) Switch voltage stress

4. Comparison

Table 1 represents the comparison of the proposed converter with previously proposed converters for the voltage conversion ratio and normalized switch voltage stress. It is clear from the table that for the same duty ratio the voltage conversion ratio of the proposed converter is greater than other with previously proposed converters. Similarly for the same voltage gain the switch voltage stress of proposed converter is lesser as compared to other previously proposed converters.

Table 1: Comparison between proposed converters and other converters

	$M = \frac{V}{V_g}$	$Ms = \frac{V_s}{V}$
Proposed converter	$\frac{2}{1-D}$	$\frac{1}{2}$
Non-inverting Zeta-derived Converter	$\frac{1+D}{1-D}$	$\frac{1+M}{2M}$
Inverting Zeta Derived Converter	$\frac{2-D}{1-D}$	$\frac{M-1}{2M}$
Type 1 Converter	$\frac{1+D}{1-D}$	$\frac{1+M}{2M}$
Conventional Cuk Converter	$\frac{D}{1-D}$	$\frac{1+M}{M}$

5. Conclusion

The study of different converters has resulted in a new switching cell. The new switching cell combines the idea of two switching cells presented in two different papers. The insertion of new switching cell in conventional Cuk converter has resulted in hybrid switch converter. The result of this new DC-to-DC converter is compared with other converters. The proposed converter has better advantages over conventional DC-to-DC converters with respect to high efficiency, high voltage conversion ratio and reduced switch voltage stress. The simulation results show full agreement with theoretical.

References

[1] Marcos Prudente, Luciano L. Pfitscher, Gustavo Emmendoerfer, " Voltage Multiplier Cells Applied to Non-Isolated DC–DC Converters," IEEE Transactions on Power Electronics, Vol.23, No. 2, March 2008.

[2] Esam H. Ismail and Ahmad J. Sabzali, "High Conversion Ratio DC–DC Converters With Reduced Switch Stress ." IEEE Transactions on Circuits and System-I: Regular Papers, Vol. 55, No. 7, August 2008

[3] Maksimovic and S. Cuk, "Switching converters with wide dc conversion range," IEEE Transaction on Power Electron., Vol. 6, Jan. 1991.

[4] Yungtaek Jang and Milan M. Jovanovic "New two-inductor Boost Converter with Auxiliary Transformer" IEEE Transaction on Power Electronics, 2002

[5] Q. Zhao, F. Tao, Y. Hu, and F. C. Lee, "Active-clamp dc/dc converters using magnetic switches," in Proc. IEEE Applied Power Electron. Conf2001,Vol.2, pp. 946–952.

[6] B. Axelrod, Y. Berkovich, and A. Ioinovici, "Transformerless DC-DC Converters with a very High DC Line-to-Load Voltage Ratio", in Proceeding .of the 2003

International Symposium on Circuits and Systems, 2003,
[7]B.xelrod, Y. Berkovich, and A. Ioinovici, "Hybrid switched-capacitor Cuk/Zeta/Sepic converters in step-up mode," in Proceeding *IEEE* Int. Symp. Circuits Syst. (ISCAS),Int. Symp. Circuits Syst. (ISCAS), Kobe, Japan, May 23–26, 2005, pp. 1310–1313.
[8] O. Abutbul, A. Gherlitz, Y. Berkovich, and A.Ioinovici, "Step-up switching-mode converter with high voltage gain using a switched-capacitor circuit," *IEEE*
Transaction Circuits and Systems Vol. 50, no. 8, pp. 1098-1102,2003
[9] Oded Abutbul, Amir Gherlitz, "Boost Converter with High Voltage Gain Using a Switched Capacitor Circuit" IEEE Transaction. on Power Electronics, 2003
[10] E. H. Ismail, M. A. Al-Saffar, A. J. Sabzali, and A. A. Fardoun, "A family of single-switch PWM family of single-switch PWM converters with high step-up conversion ratio," IEEE Transaction on Circuits and Systems May 2008.

Mr. Muhammad Saleem received B.S and M.S degrees both in Electrical Engineering from University of Engineering & Technology (UET) Peshawar, KPK, Pakistan in 2006 and 2010 respectively. From 2006 to 2009, he was Lecturer in Electrical Engineering Department at Peshawar College of Engineering, Peshawar affiliated with UET Peshawar. In 2010, he joined Electrical Engineering Department at Sarhad University of Science and Information Technology, Peshawar, KPK, Pakistan where currently he is an Assistant Professor of Electrical Engineering. His research interest areas are Power Electronics and Renewable Energy Systems.

Mr. Obaid Ur Rehman received B.S Electrical Engineering from University of Engineering & Technology (UET) Peshawar, KPK, Pakistan in 2003 and M.S degree in computing from University of Liver Pool, UK in 2006. Currently he is serving Sarhad University of Science and Information Technology, Peshawar, KPK, Pakistan as Assistant Professor.

Mr. Hashmat Khan working in the capacity of "Assistant Professor" in Electrical Engineering Department at Sarhad University of Science and Information Technology, Peshawar, KPK, Pakistan. He has more than ten years teaching as well as Research experience. His research interest areas are Power Electronics and High Voltage Engineering.