Capacitance-Voltage Analysis for Al_2O_3 based High-K Dielectric MOS Devices

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Abstract

In this paper we have calculated Capacitance-Voltage (C-V) relationship for Metal Oxide Semiconductor (MOS) devices and plotted it for high-k dielectric material Aluminum Oxide (Al_2O_3) as oxide material, Si as substrate and compared it with conventional SiO_2 based MOS device. We have made the simplest possible model for the MOS device and based on it results have been derived. The C-V characteristics are also obtained from ATLAS simulator for the MOS. Excellent agreement has been observed for theoretical and simulation results for high frequency as well as low frequency C-V curve.

Keywords: *C-V characteristics, High-k, Al_2O_3, MOS.*

1. Introduction

Attempts are being made across the world to replace the conventional silicon di-oxide (SiO_2) with different high-k dielectric materials. In this regard HfO_2 has got a lot of interest [1]. A wide study has been done on the alternative high-k dielectric materials [2]-[6]. Al_2O_3 is also one of the good candidates for it [7]-[8]. This material can allow us to reduce the size of MOS devices because it would be able to withstand higher voltages for the same gate size. The thermodynamic stability of Al_2O_3 is suitable, has high band gap energy, low leakage current and adequate value of dielectric constant. Further, Al_2O_3 gate dielectrics displayed nearly same degradation rate of capacitance reduction as SiO_2 with increment of frequency, and preserved higher k quality better than SiO_2 over a very wide range of frequency [9]. In this paper, we have obtained the C-V relationship based on the simplest possible MOS model for the high-k dielectric material Al_2O_3 and compared it for SiO_2.

2. Theoretical Formulation

Using the relation between surface potential, space charge and electric field the capacitance-voltage characteristics have been derived for a MOS structure. The potential V_0 is zero at the bulk of the semiconductor for a MOS device and at the semiconductor surface it is $V_0 = V_s$, is the surface potential. The V_0 as a function of distance can be obtained from one dimensional Poisson's equation. At the bulk of a MOS Device the total space charge density ρ (x) and V_0 being zero, the resultant Poisson's equation [10] can be written as,

$$\frac{d^2V_0}{dx^2} = -\frac{q}{\varepsilon_s}\{P_{ed}(e^{-\beta V_0} - 1) - N_{ed}(e^{\beta V_0} - 1)\} \quad (1)$$

Where q is the charge of holes, P_{ed} and N_{ed} are the equilibrium densities for holes and electrons respectively at the bulk of a MOS device, $\beta = q/kT$, k is the Boltzman's Constant, T is the temperature and ε_s is the permittivity of the semiconductor. Putting the electric field, $\xi = (-dV_0/dx)$ and integrating equation (1) toward the surface from the bulk of a MOS is,

$$\frac{1}{2}\xi^2 = -\frac{q}{\varepsilon_s \beta}[P_{ed}(-e^{-\beta V_0} - \beta V_0 + 1) - N_{ed}(e^{\beta V_0} - \beta V_0 - 1)] \quad (2)$$

Then we get,

$$\xi = \left(\frac{2kT}{q}\right)\sqrt{\left(\frac{qP_{ed}\beta}{2\varepsilon_s}\right)[(e^{-\beta V_0} + \beta V_0 - 1) + \frac{N_{ed}}{P_{ed}}(e^{\beta V_0} - \beta V_0 - 1)} \quad (3)$$

Now at the surface the electric field becomes

$$\xi_s = \pm\frac{\sqrt{2}kT}{qL_D}C$$

Where L_D is the Debye Length for holes and C is a constant with function of βV_0 and N_{ed} / P_{ed} and it is given by,

$$C = \left[(e^{-\beta V_0} + \beta V_0 - 1) + \frac{N_{ed}}{P_{ed}}(e^{\beta V_0} - \beta V_0 - 1)\right]^{1/2} \quad (5)$$

Now, from Gauss's law (or unit volume, $\int dV = 1$) the space charge per unit area is

$$Q_{space} = -\frac{\sqrt{2}\varepsilon_s kT}{qL_D}\sqrt{[e^{-\beta V_0} + \beta V_0 - 1 + \frac{N_{ed}}{P_{ed}}(e^{\beta V_0} - \beta V_0 - 1)]} \quad (6)$$

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Where, ε_s is the permittivity of the semiconductor for the device. Then the differential capacitance at the depletion layer of MOS is,

$$C_D = \frac{dQ_{space}}{dV_0} = \frac{\varepsilon_s}{\sqrt{2}L_D}\frac{\left((1 - e^{-\beta V_0}) + \frac{N_{ed}}{P_{ed}}(e^{\beta V_0} - 1)\right)}{C} \quad (7)$$

When a potential is applied across a MOS structure the charges in oxide and semiconductor layers align themselves so as to resemble a capacitor. Now the capacitance of the system depends upon the frequency of applied electric field. As pointed out earlier the capacitance of the oxide layer does not depend upon the applied potential and is fixed depending upon its dielectric permittivity and the geometry. But in the semiconductor layer the effective width over which the charges are there changes with applied potential. Depending upon the polarity of the applied potential either majority or minority charge carriers have to move towards the surface or away from it.

3. Result and Discussions

With external applied voltage the majority carriers can respond immediately but for minority carriers the response time is more. If the applied potential changes so quickly that the polarity across the MOS changes before the minority carriers could respond to the applied field, the applied field is said to have a high frequency. On the otherhand if minority charges carriers are able to respond to the applied filed and then the polarity is changed then the frequency of the applied field is said to be low.
Let us consider a pMOS, try to understand what will happen by applying an AC voltage across MOS and obviously the arguments for nMOS will be exactly similar except to as the polarity of the applied bias and the nature of the majority and minority charge carriers. In the negative half cycle when the magnitude is sufficiently large the maximum possible majority charge carriers get accumulated near the oxide semiconductor surface and the capacitance reaches its maximum value. As the magnitude of the applied potential decreases, proportionally the accumulation decreases and there is no effect on the capacitance of the semiconductor layer. But as the magnitude of potential gets closer to zero, the mutual repulsion between the majority charge carriers also become important. And the accumulated charge decreases faster than the applied potential decreases. At zero applied potential still holes are there in majority and there is a finite capacitance. Now when the potential becomes positive majority charge carriers will be gradually repelled and the minority charge carriers come towards the surface. These results in decrease in charge till both of them become equal in density near the surface. At this point the capacitance is a minimum. Now as the positive potential is increased further inversion begins to take place and capacitance increases. Finally it reaches its maximum value after which it remains constant. Now as we made the model for our low frequency electric field, we can claim that all the formula derived for the static potential case will be valid in this case too, except that the potential will vary with time. So our set of equations is,

$$C_D = \frac{dQ_{space}}{dV_0} = \frac{1}{2}\frac{\sqrt{2\varepsilon_s kT}}{qL_D}\frac{\sqrt{\left[-\beta e^{-\beta V_s} + \beta + \frac{N_{ed}}{P_{ed}}(\beta e^{\beta V_s} - \beta)\right]}}{C} \quad (8)$$

The voltage applied across the MOS system distributes across the oxide layer and semiconductor i.e.

$$V(t) = V_s(t) + \frac{Q_s}{C_I} \quad (9)$$

Now C_I is fixed because none of the parameters controlling it has changed but V_s changes with time. So C_D also changes because it is controlled by V_s and the net capacitance of the system also changes. So,

$$\frac{1}{C} = \frac{1}{C_{ox}} + \frac{1}{C_D} \Rightarrow \frac{C}{C_{ox}} = \frac{C_D}{C_D + C_{ox}} \quad (10)$$

For SiO_2 and Al_2O_3 the low frequency behavior is plotted in figure 1.

As already said high frequency would mean that minority carriers don't get sufficient time to do the best. Certainly if the frequency applied is so high that it doesn't even allow majority charge carriers to respond, then the following arguments and hence the derived equations won't be valid anymore. But by developing a mathematical model we can come to the conclusion that frequency till what we usually apply practically, majority charge carriers respond almost instantaneously. So the arguments till the minimum capacitance is reached remains the same as it was in the low frequency behavior (because it is decided by the majority charge carriers). After it since the minority carriers can't respond with changing rate of field there would not be any rise in the capacitance (see figure 2). Then the equations become:

$$C_D = \frac{dQ_{space}}{dV_0} = \begin{cases} \frac{1}{2}\frac{\sqrt{2\varepsilon_s kT}}{qL_D}\frac{\left[1 - e^{-\beta V_s} + \frac{N_{ed}}{P_{ed}}(e^{\beta V_s} - 1)\right]}{C} & \text{if } V_s < V_j \\ \frac{1}{2}\frac{\sqrt{2\varepsilon_s kT}}{qL_D}\frac{\left[1 - e^{-\beta V_j} + \frac{N_{ed}}{P_{ed}}(e^{\beta V_j} - 1)\right]}{C} & \text{if } V_s \geq V_j \end{cases} \quad (11)$$

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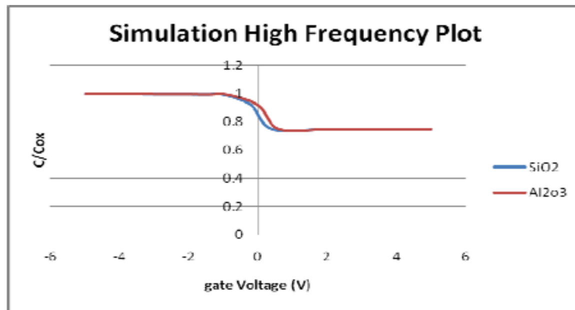

Fig. 1 Low frequency curve.

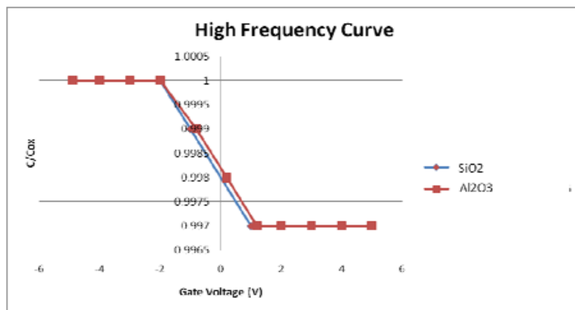

Fig. 2 High frequency curve.

The change in relative capacitance of MOS with Al_2O_3 as the gate material is for larger value of gate voltage than for MOS with SiO_2. The transition region starts at more positive value of gate voltage than in SiO_2 based MOS. This is because of the capability of Al_2O_3 to withstand more electric field as discussed earlier. Thus it can be said that the stability of MOS structure has increased.

The MOS device with SiO_2 and Al_2O_3 as the oxide material, alternatively are modeled and simulated with ATLAS simulator for low frequency (see figure 3) as well as high frequency (see figure 4). The variation C/C_{ox} with the gate voltage as the independent parameter shows the some variation as obtained with the theoretical modeling of the MOS device used in this paper.

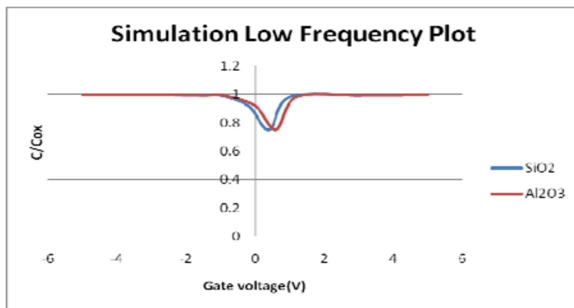

Fig. 3 Low frequency curve (simulated).

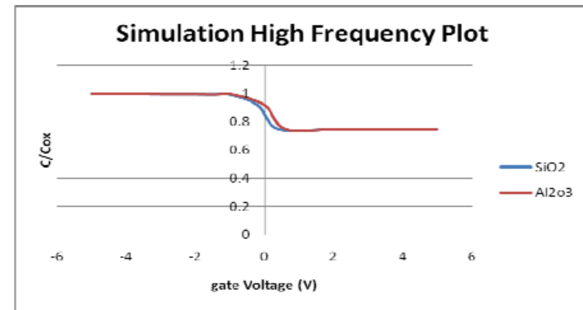

Fig. 4 High frequency curve (simulated).

The minimum capacitance of the simulated curve is less than that of the theoretical, which is due to the effect of the capacitance due to the fast interface charge density. That is incorporated by the simulated result, and appears in parallel combination with depletion capacitance at the insulator-semiconductor interface. Hence Al_2O_3 is having a high-k value, the same electrical characteristics as that of a MOS device with SiO_2 as the insulator material, can be obtained with a greater thickness of Al_2O_3, hence reducing the leakage current considerably.

4. Conclusions

The theoretical study revealed that even a very simple model can be used for the study of complex devices like MOS. Almost identical transitions in C-V are observed theoretically as well as simulation with the gate dielectric materials, showing better reliability of Al_2O_3 with significant reduction of tunneling leakage current. The higher thickness of Al_2O_3 also results in lesser leakage current. The only major problem is the interfacial property of the Si-Al_2O_3.

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