Indigenous Patch Clamp Technique: Design of highly sensitive amplifier circuit for measuring and monitoring of real time ultra low ionic current through cellular gates

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Abstract

The importance of Noble prize winning "Patch Clamp Technique" is well documented. However, Patch Clamp Technique is very expensive and hence hinders research in developing countries. In this paper, detection, processing and recording of ultra low current from induced cells by using transimpedence amplifier is described. The sensitivity of the proposed amplifier is in the range of femto amperes (fA). Capacitive-feedback is used with active load to obtain a 20MΩ transimpedance gain. The challenging task in designing includes achieving adequate performance in gain, noise immunity and stability. The circuit designed by the authors was able to measure current in the range of 300fA to 100pA. Adequate performance shown by the amplifier with different input current and outcome result was found to be within the acceptable error range. Results were recorded using LabVIEW 8.5® for further research.

Keywords: *drug discovery, ionic current, operational amplifier, patch clamp*

1. Introduction

Biochemists have reported the importance of ionic channels, especially for drug discovery. It is imperative to understand the mechanism by which ionic channels, play the role of cellular gates. Newly discovered drugs need to be compatible with these cellular gateways to allow them to be incorporated. Biochemists had deciphered the amino acid sequences of Na^+ channels (M. Noda *etal*., 1984), and biophysicists had revealed single-channel properties with patch clamp techniques (B. Sakmann and E. Neher, 1983). The hybrid of biochemistry and biophysics has a lot of potential to generate unprecedented information pertaining to cellular structure and function (M. Mishina *etal*., 1985; M.M. White *etal*., 1985).Molecular motions of channels have been modeled to understand the influences of ion transport via time-dependent fluctuations. Studies should be geared towards understanding the permeation of drugs via a narrow pore where ions approach channel walls.Cells house a variety of ionic channels, which are complex. These channels are funnel- shaped vestibules which lead to selective narrow regions deeper in the pore. These channels include the Na^+ channels; the acetylcholine receptor channels (AChR), the K^+ channels and the Ca^{+2}-dependent K^+ channels (R. Latorre and C. Miller, 1983; B. Hille, 1984).The molecular mechanics of ionic channels is quite complex. The AChR has an opening of 11 nm long, with a 2.5 nm outer entrance and a 1.5 nm inner entrance (A. Brisson and P.N.T Unwin, 1985). The pore which is lined by hydrophilic amino acids also includes many charged ions,

giving the channel a small but overall net charge. These ions flow due to a strong influence of a membrane potential.

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The permeation of drugs includes many factors which are; binding of the drug, net protein charge, dipoles, molecular properties of water, ion and channel site hydrations, thermal fluctuations of proteins and steric hindrances.
This study was directed to address the above challenges, and to deeply understand the molecular interactions going on in the cellular gates. If this plethora of ions is understood, drug discovery could be facilitated. The pharmaceutical industry has widely recognized patch clamping as the "gold standard" to provide the highest information content in the drug discovery screening process by directly measuring the current passing through ion channels (A. Brueggemann, 2004; B. Sakmann and E. Neher; 1983).
The patch clamp technology, developed 30 years ago by German researchers Neher and Sakmann, allows direct voltage control of a cell and thus the ability to study ion channels in detail for pharmaceutical studies (M. Karmažínová and L. Lacinová, 2010; D. Ogden and P. Stanfield, 1994). Patch clamp is a very high resolution technique, supplying both high quality data and high information content as depicted by Y Zhao *et al*. in 2009 (Y. Zhao *etal*., 2009). Despite these advantages it remains a low efficiency technique such that even a skilled patch clamper can record data from only 20-30 cells during an 8-hour work day (C. Hesketh, 2009). In response to this major limitation, customized designs have been developed for patch clamp systems which are easy to handle, user friendly and cost effective.

2. Hardware Description

As depicted by Erwin Neher and Bert Sakmann's article on patch clamp apparatus (E. Neher and B. Sakmann, 1976) and the latest advancement on this technique, a normal patch clamp system should consist of an Inverted Microscope with a camera, two electrodes, a voltage supply, an amplifier unit, ADC (analog to digital converter), Micro Controller for serial data transmission and a software which runs on computers. A typical setup of Patch Clamp Technique is shown in Fig. 1.
In a simple patch clamp technique, both electrodes are directly attached with the cell membrane (B. Sakmann and E. Neher, 1984) and shown in Fig. 1.When a pulse is applied from the pulse generator through "Electrode 1", the movement of ions takes place which is detected by "Electrode 2". Hardware description of each part is given below:

2.1 Microscope
Nikon® inverted microscope (TS-100F) is used to observe living cells

2.2 Voltage Supply
Dual voltage supply is used to power up the circuit. The dual voltage supply has been developed in-house.

2.3 Pulse Generator
The rate of opening the channels and magnitude of voltage is controlled through a pulse generator (J.V. Halliwell *etal.*, 1994).

2.4 Electrodes
The first electrode is used to generate voltages up to milli volts which open the gates of ionic channels. The second electrode is connected to a BNC (Bayonet Neill-Concelman) connector through direct pipette holder plugs. The center pin of the BNC connector is the input of the amplifier's main unit.

2.5 Amplifier Unit
Self constructed amplifier unit contains op-amp (operational amplifier) circuitry for processing the incoming signal.

2.6 Analog to Digital Converter (ADC)
To convert continuous signals into discrete forms, an analog to digital converter is used.

2.7 Software
In-house made software on LabVIEW 8.5® is used with the hardware, which shows results on a PC in the form of graphs.

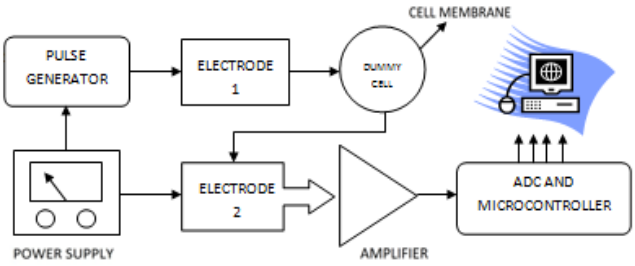

Fig. 1. Typical setup of Patch Clamp Technique.

3. Experimental Procedure

The proposed circuit is capable of handling 300fA to 100pA. As the input current is ultra low, in order for it to be processed we have to first amplify it. The output signal from the amplifier circuit is in the range of 0V to 2.56V. To digitize the input current, 10 bits ADC is used for high resolution, so that the least possible change can be detected (N. Gray, 2006; J.R. Drummond, 1997). Programming is done on ATMEL AVR® (modified Harvard architecture 8-bit RISC, reduced instruction set computing, single chip microcontroller) for transmitting data serially into the computer (A.V.R. Atmel). The controller is then programmed using BASCOM® (C. Kuhnel, 2003). RS232 port is used for serial data communication (J.G. Ganssle, 1995) which is further processed through software. Specialized software is designed in LabVIEW 8.5® which shows the final results in the form of graphs and also records data. The bit that was received by the software is first

converted into numeric format for performing calculations on it. The mathematical operators are then used to nullify gain, changing voltage into current and implementation of arrays for viewing current in the form of graphs. As this technique is used for research purpose, the recording option is also provided in the software which stores data in MS EXCEL® (2007).

4. Amplifier Circuit

An amplifier circuit is used to measure electric signal current, which is typically in the range 300fA to 100pA which is generated from living cells (G. White *etal*., 1989).

The device used in the proposed circuit is an ultra-low-noise, ultra-low input bias current as shown in Fig. 2, coupled with an operational amplifier (OP80), manufactured with metal oxide silicon (MOS) technology input stage (L. Zhang etal., 2010; R.R. Harrison and C. Charles, 2003).

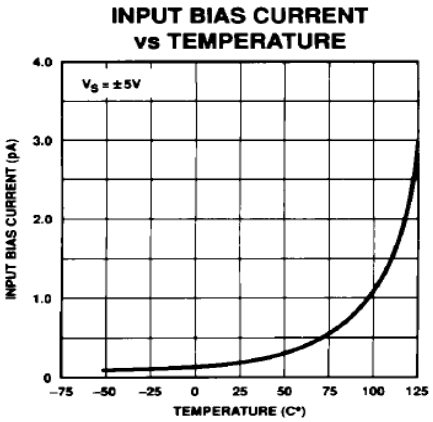

Fig. 2. Graph depicting the relationship between input bias current and temperature of OP80.

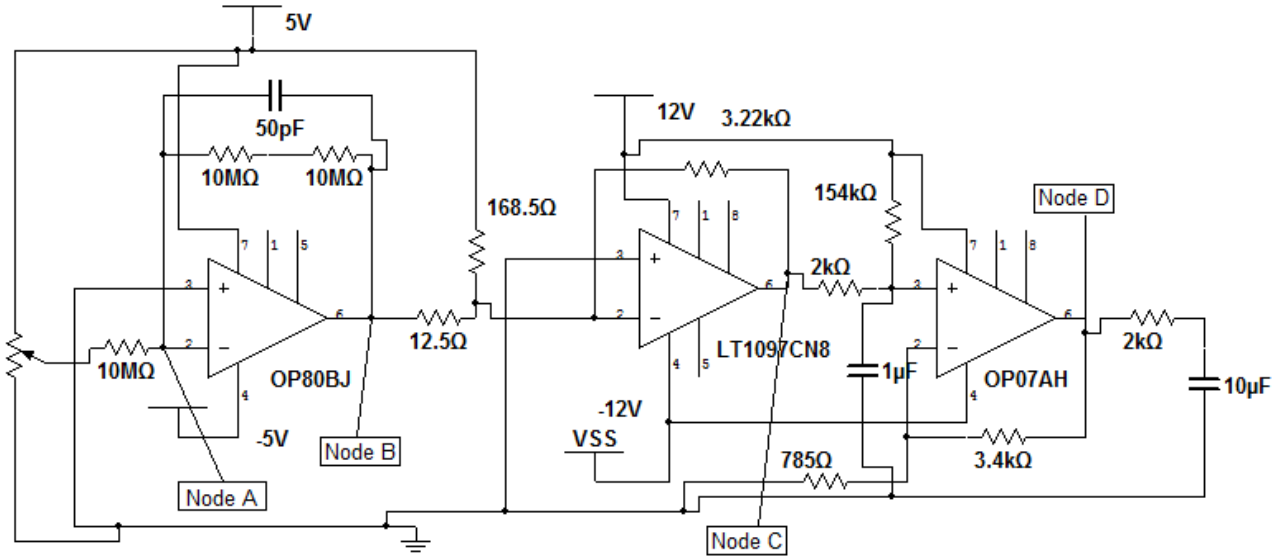

Fig. 3. Circuit diagram of sensitive amplifier for DC ion current detection..

It has one of the lowest input bias current operations available in the local market, and is guaranteed by the manufacturer (Analog Devices®) after extensive testing at around 150×10^{-15}A.

Moreover, it offers superior noise performance, tested by the manufacturer at 70nV/√Hz @ 1kHz input voltage noise (Analog Devices, 2010). The schematic presentation of an electrometer circuit for DC ions detection is shown in (Fig. 3). In this circuit, current is converted into voltage at the initial stage by using transimpedence amplifier (H. Hashemi, 2002; P. Intra and N. Tippayawon, 2009) to avoid interferences, and then amplification of voltage is done. At the end of the circuit, low pass filter is placed to nullify RF (radio frequency) noise which adds to the signals during processing.

The circuit adopts two cascaded negative feedback and one positive feedback amplifiers. Gains of each state amplifier (A.S. Sedra and K.C. Smith, 2004; W. Storr, 2010) are calculated using following formulae:

$$V_{out} = -I_{in}R \quad (1)$$

$$V_{out} = -(R_2/R_1)V_{in} \quad (2)$$

$$V_{out} = (1 + R_2/R_1)V_{out} \quad (3)$$

A 12V DC power supply capable of providing 200mA is required. Analog Devices report that to cancel the effect of input capacitance, the pole created must be neutralized by a

zero that is located at the same frequency as shown in Fig. 4 (Analog Devices, 2010).

To introduce this zero, the capacitor is placed around the feedback resistor with the value such that:

$$1/R_1C_1 2\pi \geq 1/R_2C_f 2\pi \quad (4)$$

$$R_1C_{in} \leq R_2C_f \quad (5)$$

RC (resistor capacitor), a low-pass filter blocks high-frequency noise and allows low frequency signals to pass through it, prevents oscillations of the amplifier output (A.S. Sedra and K.C. Smith, 2004) which was designed for ultra-low current measurement and featured ultra-low input bias current and low offset voltage drift. This circuit gives maximum output voltage of 2.56V at 100pA of input signal current.

Masroor Hussain Shah Bukhari, John H. Miller Jr. and Zahoor Hussain Shah (M.H.S. Bukhari *etal*., 2009) took special care to minimize the current leakage and noise in the amplifier circuit during the processing of the signal, which basically includes short noise and thermal noise.

Bob Pease proposed some remedies to save ultra low current from noise which included, fabrication of the amplifier on Teflon material or polyimide if the highest precision was needed (B. Pease, 1993).

A significant reduction in electromagnetic noise was observed by placing the whole circuit in a ground connected box which absorbed the external interferences.

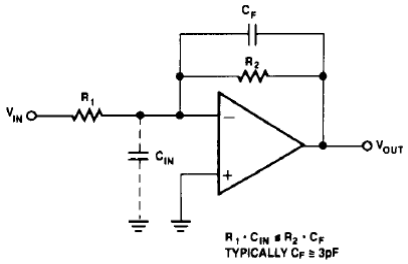

Fig. 4. Cancelling the Effect of Input Capacitance.

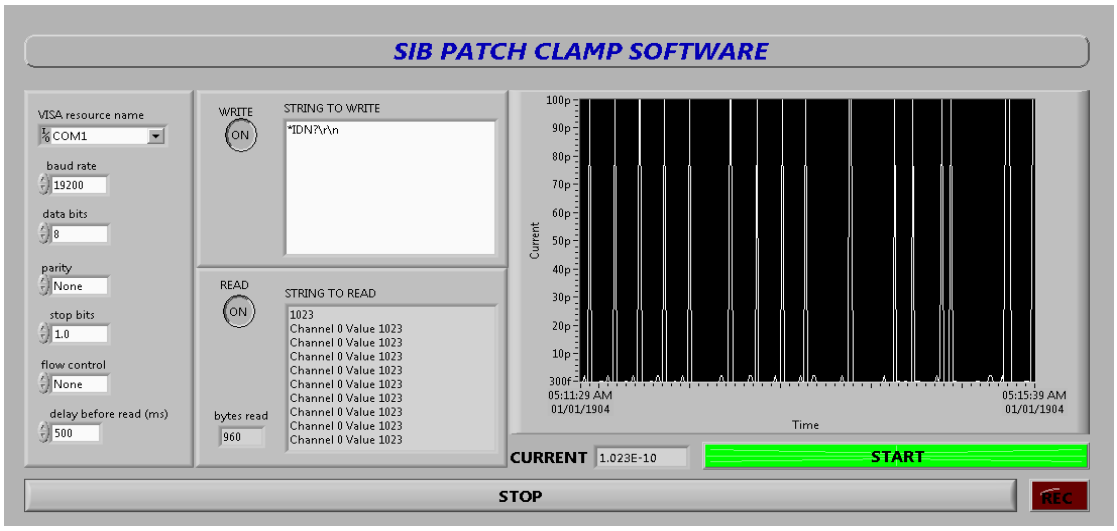

Fig. 5. In-house design Patch Clamp Software front panel.

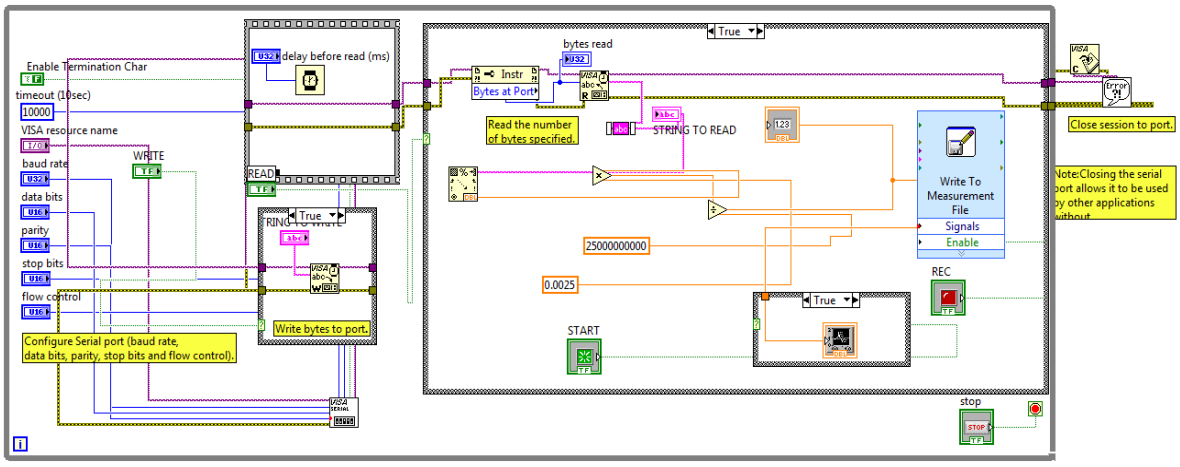

Fig. 6. In-house design Patch Clamp Software block panel.

For optimal amplifier operation 0.1µF/10µF bypass capacitor was added to the supply pin, and subsequently more capacitors were added on the path of V_{DD} (voltage drain-drain). The 0.1µF was used to bypass high frequency noise and 10µF was to keep power source stable (Samsung Electronics Co. Ltd, 2008). Shielding wires and guard rings were introduced around the input terminals of op-amp to eliminate the surface leakage current and common mode signals.

To make the unit clean and free of any deposition or contamination it was washed with a solution of 85% ethyl alcohol (C_2H_5OH) (B. Lang, 1998), wiped dry with high-pressure clean air and then treated in an ultrasonic bath (M.H.S. Bukhari etal., 2009).

5. Software Design

The software was designed to give GUI (graphical user interface) to the users. Fig. 5 and Fig. 6 show the front panel and block diagram of designed software. The front panel includes chart, string palette, numeric palette and buttons for start/stop and for recording the operation.

A VISA Configure Serial Port® panel is used to receive serial data. The data received by the software is in string format, to perform mathematical operations and to show results on a chart, the data is first converted into numeric format.

To show a continuous graphical result; a chart is used instead of a graph for continuous data retrieval as explained in the LabVIEW tutorial 8.5 (NI Developer Zone, 2010; National Instruments, 1996).

6. Results And Discussion

The overview of patch clamp technique and demonstration of ultra-low current meter has been described in this paper. Through this meter we are now able to measure current in the range of 300 fA to 100 pA.

TABLE 1: FIRST STAGE AMPLIFICATION BY USING TRANSIMPEDENCE AMPLIFIER

Input Current (pA)	Calculated Voltage (mV)	Observed Voltage (mV)	Error (%)
10	-0.2	-0.3	50
20	-0.4	-0.5	25
30	-0.6	-0.7	16.6
40	-0.8	-0.9	12.5
50	-1	-1.0	0
60	-1.2	-1.4	16.6

TABLE 2: SECOND STAGE AMPLIFICATION BY USING INVERTING CONFIGURATION

Input Voltage (mV)	Calculated Voltage (mV)	Observed Voltage (mV)	Error (%)
-0.3	77.4	88.3	14.08
-0.5	129	116.8	9.4
-0.7	180.6	194	7.4
-0.9	232.2	245	5.5
-1.0	258	270	4.6
-1.4	361.2	365	1.05

TABLE 3: THIRD STAGE AMPLIFICATION BY USING NON-INVERTING CONFIGURATION

Input Voltage (mV)	Calculated Voltage (V)	Observed Voltage (V)	Error (%)
88.3	0.441	0.45	2.04
116.8	0.584	0.62	6.16
194	0.97	0.94	3.09
245	1.225	1.23	0.4
270	1.35	1.33	2
365	1.825	1.6	12.3

The Tables I, II, III shows the results of individual stages of amplifier circuit along with the percentage error range.

The tables show the induced input current from a dummy cell ranging from 10pA to 60pA and after amplification from each stage, the corresponding voltage is observed using a voltmeter. The current is generated by placing a 10MΩ resistor in series with a potentiometer having biased with 5V as it enters the circuit through Node A.

In the first stage the voltmeter was placed between Node B and Ground to check the amplification of 30pA current in terms of voltage from OP80 and it was found to be -0.7mV.

The calculated value was -0.6mV giving an error of 16.6% which was acceptable. In the second stage, LT1097 was used. -0.7mV was taken as an input voltage and the amplified voltage was observed between Node C and Gnd. The observed value was 194mV instead of 180.6mV with a percentage error of 7.4%. Non inverting configuration was through OP07 which was used at the final stage to get a positive output voltage. With a gain of 5 times, 194mV was amplified up to 0.94V with an error of 3.09% at Node D.

The comparison of observed values with the calculated ones is shown in Fig. 7. X-axis represents the input ionic current from the induced cell and Y-axis shows the corresponding amplified voltage through op-amp. The plot from the ideal value is a straight line as the gain is constant. However, the curve that forms through the observed values is not a straight line because of some error and interfering noise. The error was probably due to the tolerance (5%) of resistors, short noise and thermal noise. Ideally the tolerance of resistors should be neglected; however, there was a significant effect of the resistors due to temperature changes which was reduced by performing the experiment at constant environmental temperature i.e. 20°C. The other affects of error were contributed due to the internal I.C`s noise which came into effect as the frequency of the input signals increased. As depicted in the graph, the curve which forms with the observed value is away from the ideal line in the initial stages, as the current is ultra low and when the current increases, the observed value line gets close to the ideal one. This abnormal behavior of amplifier circuit is due to the interfering noise, which effects when the current is ultra low and produces the greater effect.

7. Conclusion

The purpose of this research was to indigenize patch clamp apparatus in Pakistan and other developing countries. The ultra low current detector is the core part of this technique.

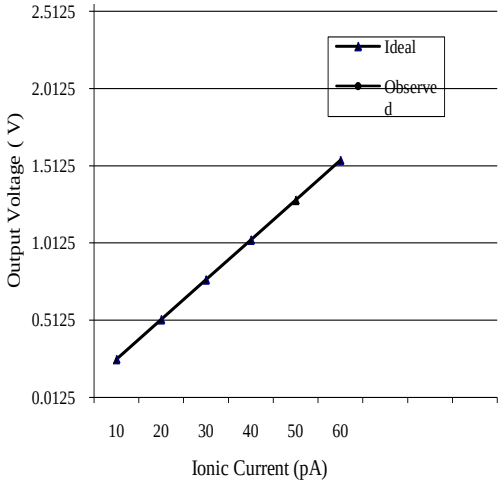

Figure 7. Typical setup of Patch Clamp Technique.

The amplifier was designed in such a way that the components used are easily available in the local market. For example, use of Giga Ohm Resistors, as used by M. H. S. Bukhari, John H. Miller Jr. and Zahoor Hussain Shah in 2009 (M.H.S. Bukhari *etal*., 2009), completed the circuit in a single stage but as it was not available in local markets so to avoid unavailability of such equipments, different tactics have been applied. This is the first time such an approach has been used in Pakistan to indigenize an electrophysiological technique because in a developing country like ours, it is very difficult to import such equipment which costs around Rs 20million. In a broad picture, indigenization of such type of techniques with economical rates will increase our research capabilities.

Future prospects include understanding how large electro-potential gradients across membranes affect diffusion of drugs. It is imperative to employ the indigenized patch clamp

apparatus to study the behavior of size, shape, net charge and binding of drugs with the cellular gates.

8. Acknowledgment

I am very thankful to Faisal Khan for providing hands-on training on Patch Clamp Apparatus which became very beneficial for me in theoretical point of view.
From Ejaz Ahmed, Ayaz Ahmed and Sarmad Hameed, I learned about the technical challenges faced during amplifier design and hardware compatibility.

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